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NOTES:
1.HSF Property:Comply iSupplier system HSF property attribute up-to-date value.

THRONE
15KBL MD U22 & R U42
SVT BUILD
2017.08.09

18-Apr-2017		
DATE	CHANGE NO.	REV

DESIGN / DRAWER	XXX	DATE	18-Apr-2017
CHECK	BRYAN CHIOU		
APPROVAL	TICKY TSAI		
FILE NAME	R10_TOPAZ_WS		
PCB PN	6050A2940901	PCB VER	A01

INVENTEC			
TITLE Throne R15			
SIZE A1	COLOR G	DRAWING NUMBER 1310xxxxx-0-0	REV X01
SHEET		of 24	

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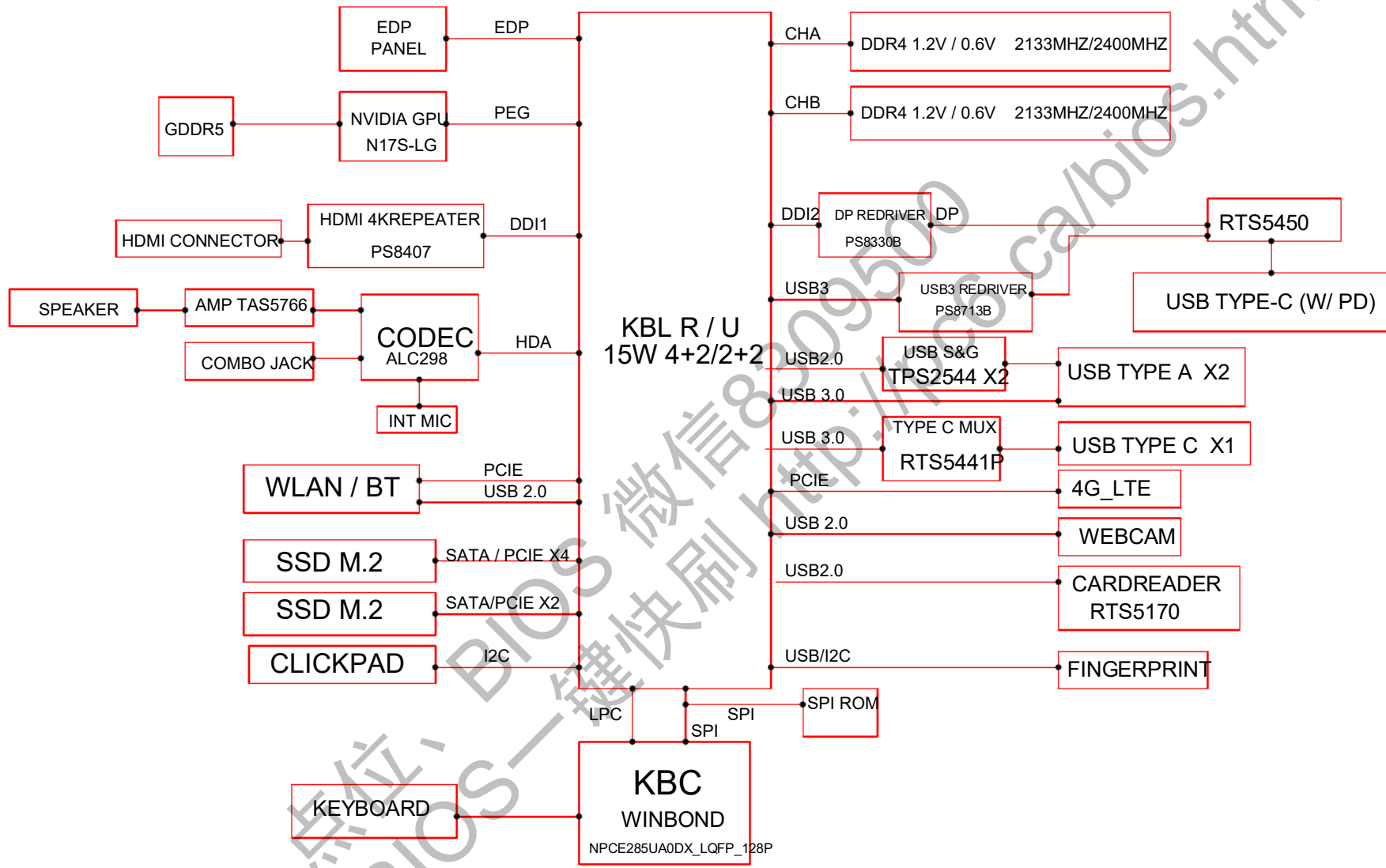
26 CPU-DDR
27 CPU-LPC, SPI, SMBUS, CLINK
28 CPU-GPIO
29 CPU-MISC, HDA, SDIO, JTAG
30 CPU-PCIE, USB3, USB2
31 CPU-CLK, RTC, CFG
32 CPU-DDI, EDP, CSI2, EMMC
33 CPU-POWER MANAGEMENT
34 CPU-POWER1
35 CPU-POWER2
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45 USB3.0 CONN1
46 USB3.0 CONN2
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48 TYPE C RTS5441P
49 TYPE C CONN1
50 WLAN ON BOARD
51 4G_LTE
52 NGFF_M.2 SSD1

53 NGFF M.2 SSD2
54 DP REDRIVER
55 USB3 REDRIVER
56 TYPE C RTS5450
57 TYPE C CONN2
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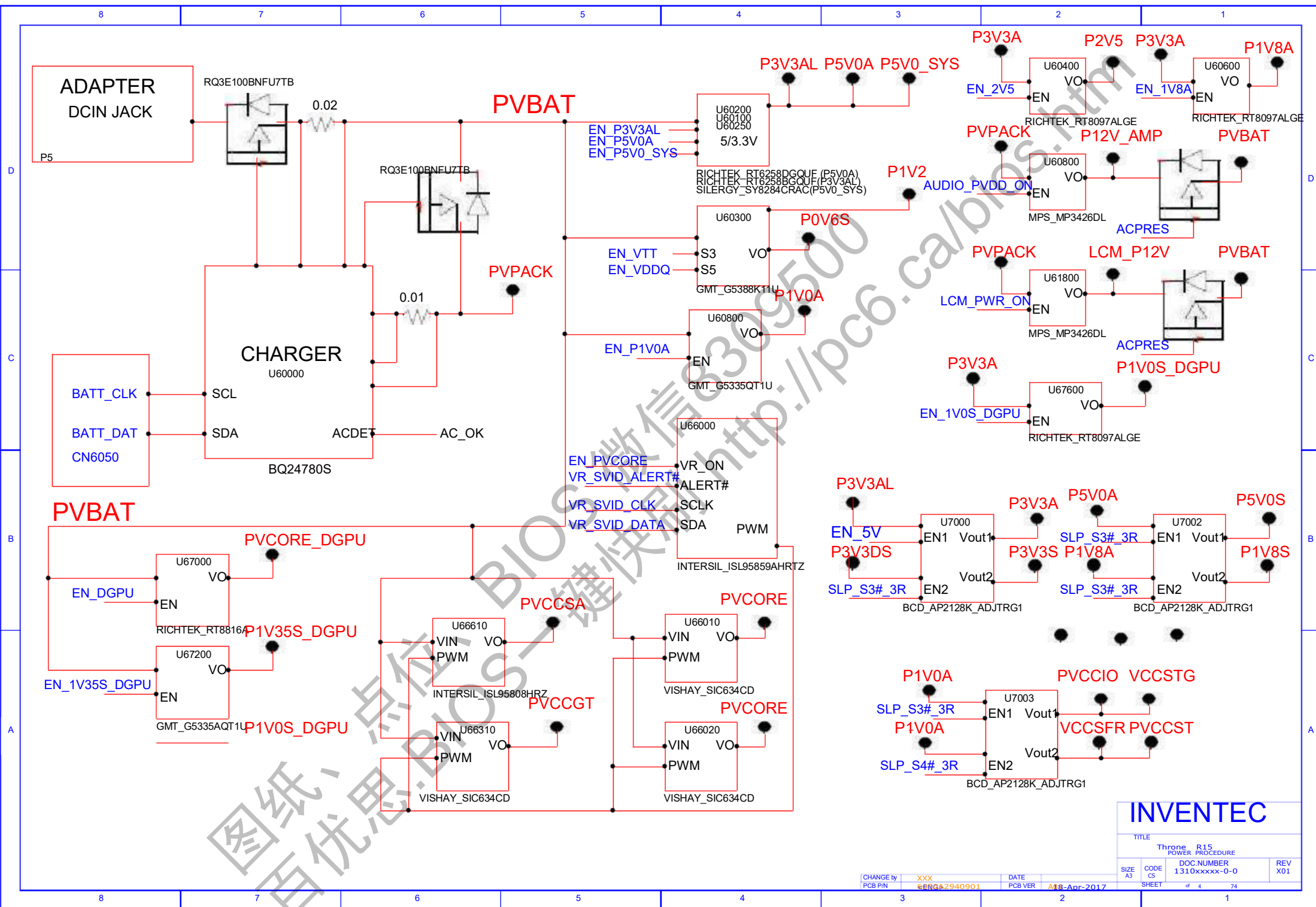
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SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET of 2 74			

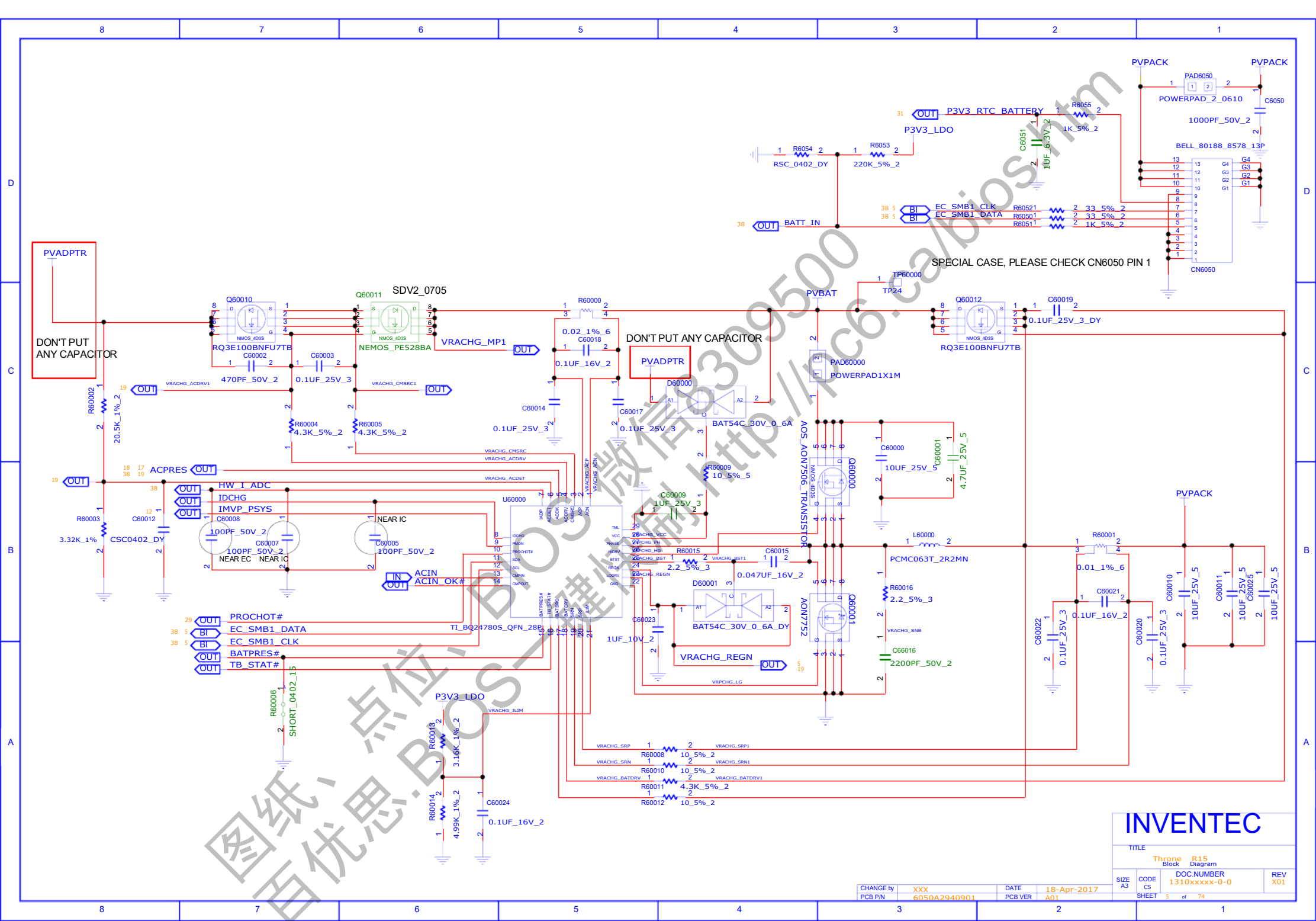
CHANGE by PCB PIN	XXX 6650A2940901	DATE PCB VER	A08-Apr-2017
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INVENTEC				
TITLE				
Throne R15 Block Diagram				
SIZE	CODE	DOC NUMBER	REV	
A3	CS	1310xxxx-0-0	X01	
SHEET	3	of 74		

CHANGE by	XXX	DATE	18-Apr-2017
PCB P/N	6050A2940901	PCB VER	A01

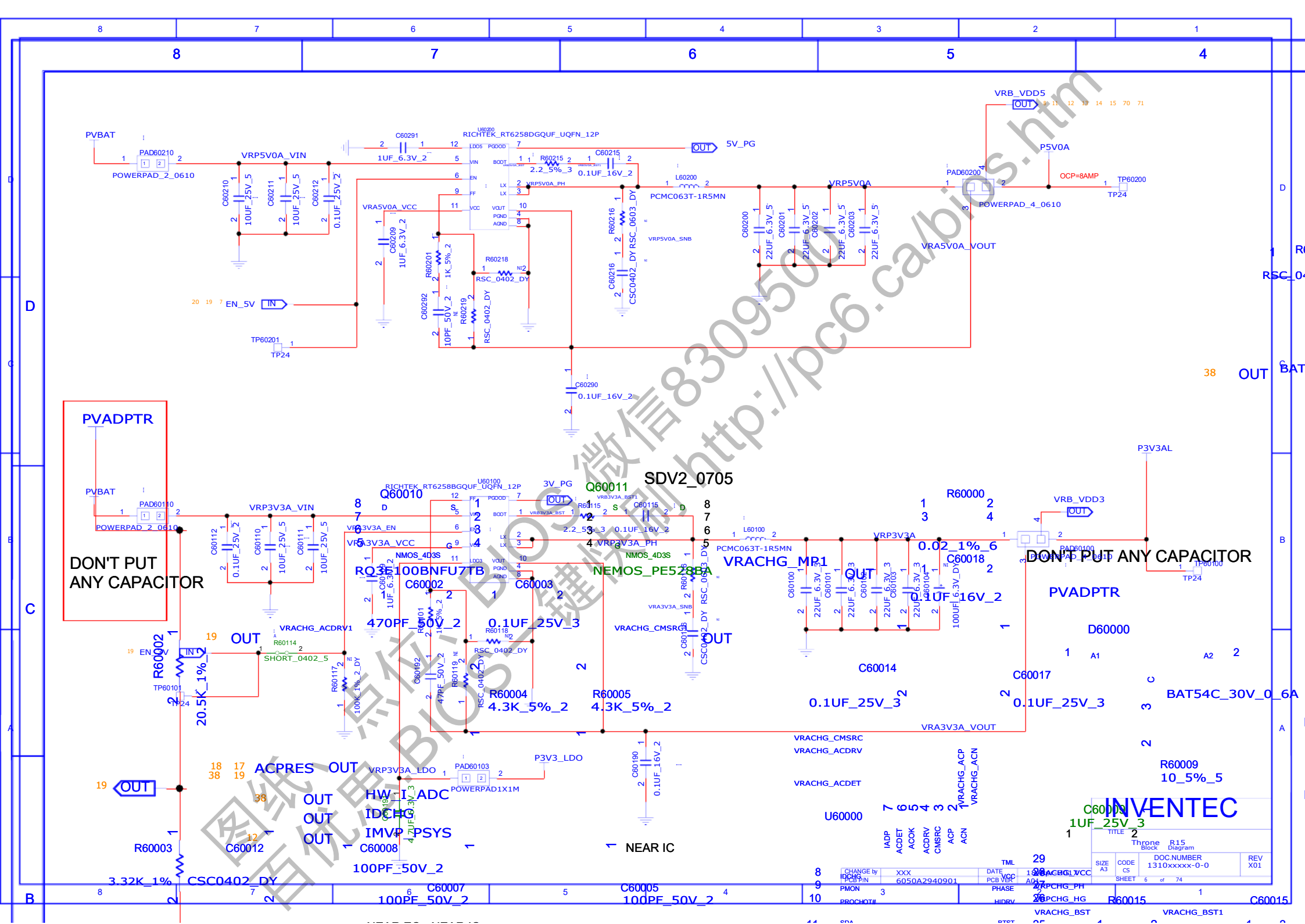


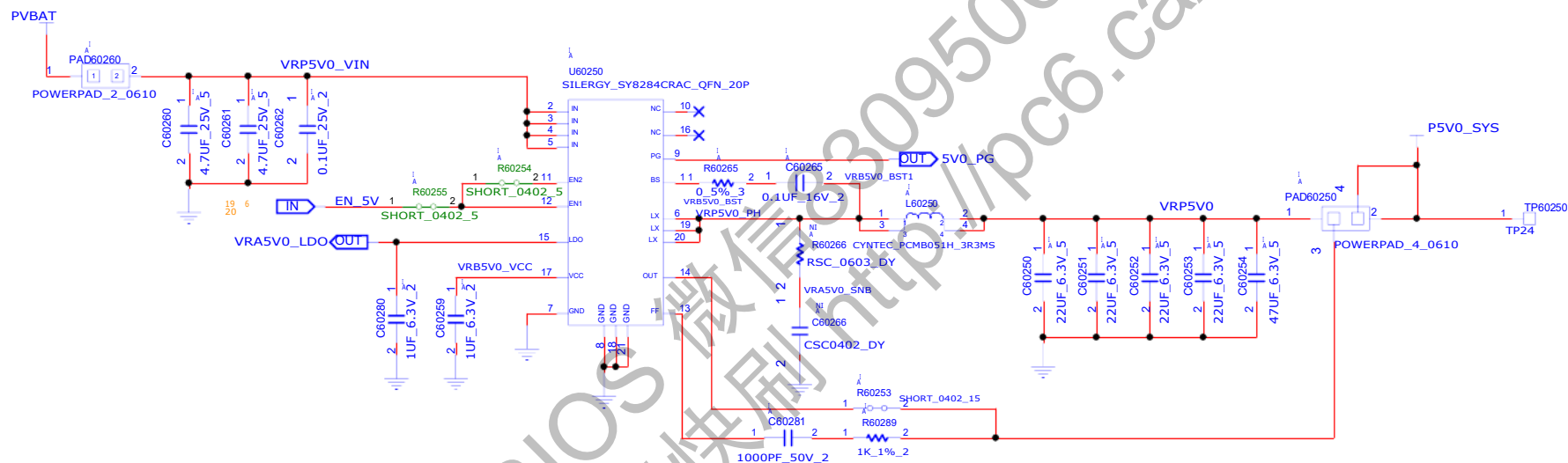


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A3	CS	1310xxxx-0-0	X01
SHEET	5	of 74	

CHANGE by	XXX	DATE	18-Apr-2017
PCB P/N	6050A2940901	PCB VER	A01





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TITLE
Throner_R15
Block
Diagram

SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01
SHEET 7		of 74	

CHANGE by PCB P/N	XXX 6050A2940901	DATE PCB VER	18-Apr-2017 A01
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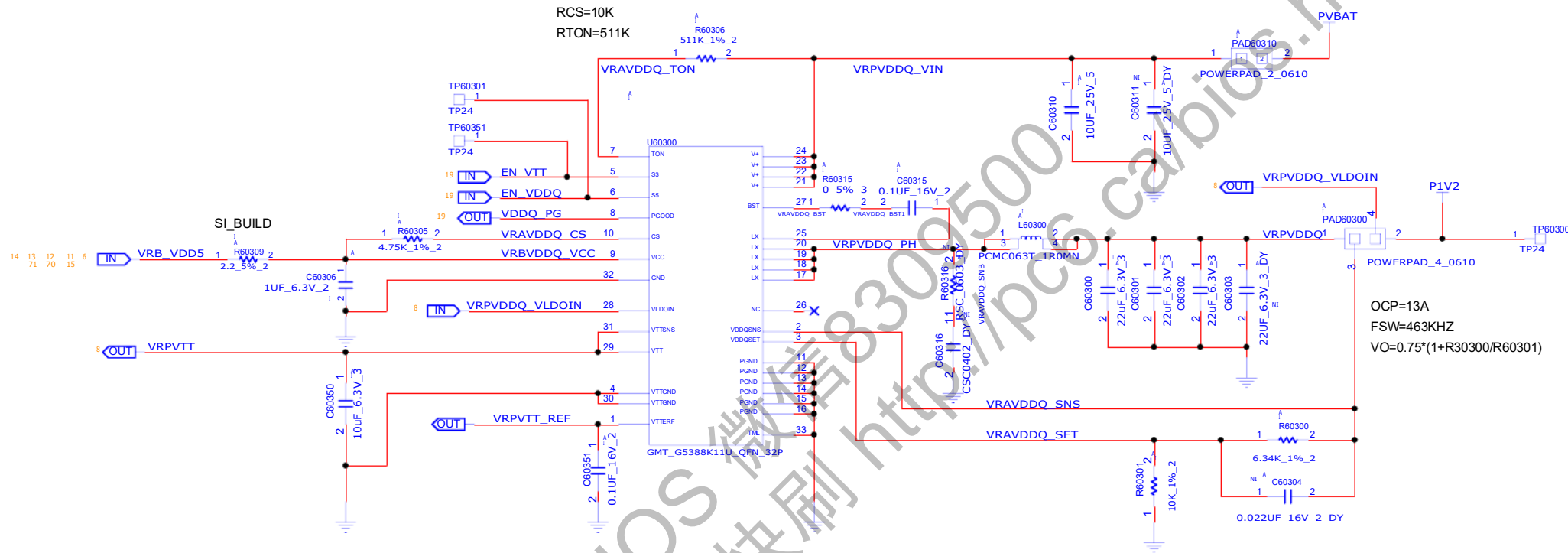
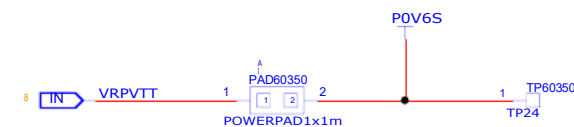
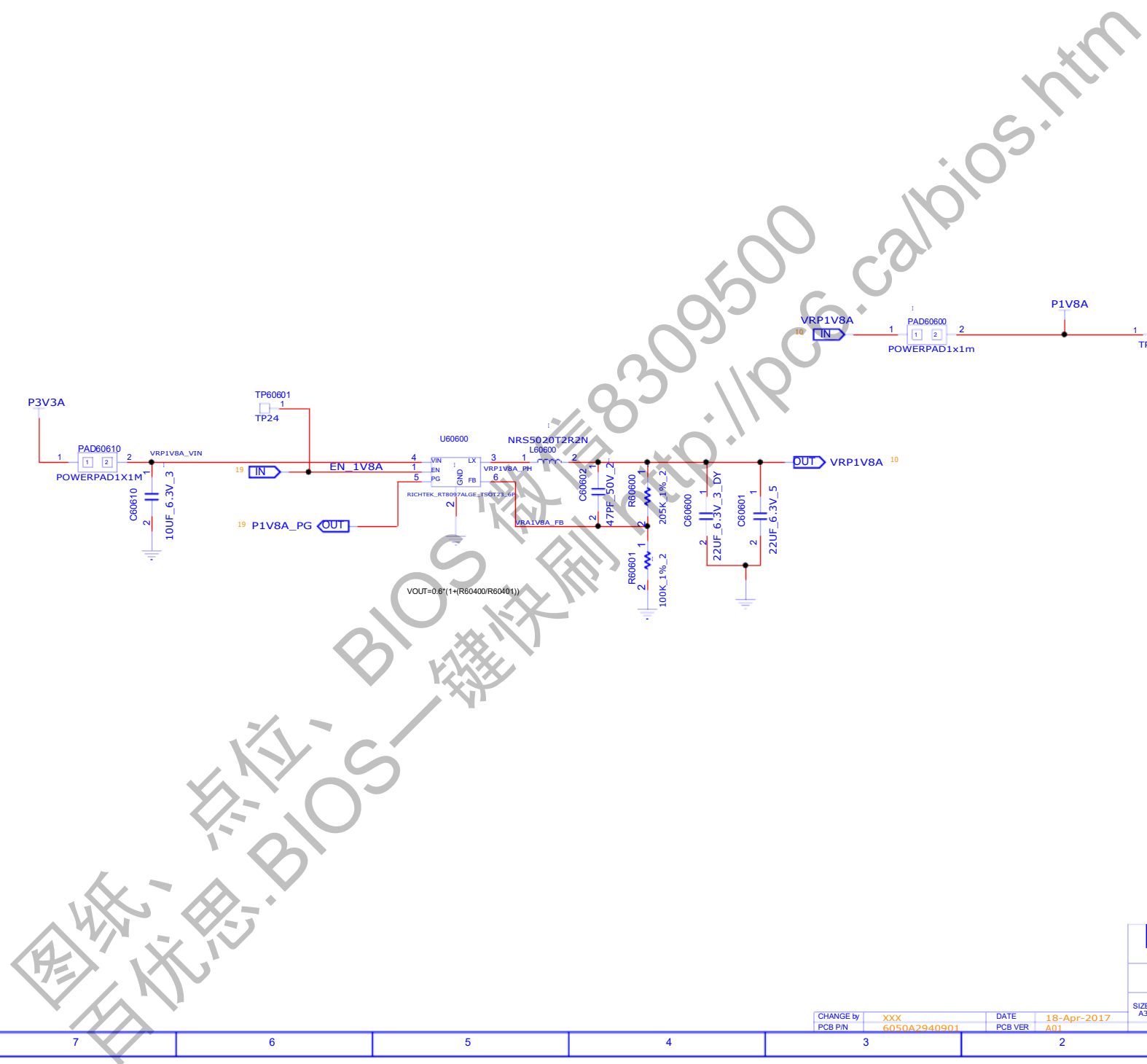


Table 2. S3 and S5 Control Table

STATE	S3	S5	VTT	VTTREF
Normal	Hi	Hi	VTTREF	VDDQSNS/2
Standby	Lo	Hi	OFF (High-Z)	VDDQSNS/2
Shutdown	Lo	Lo	0V (Discharge)	0V (Discharge)



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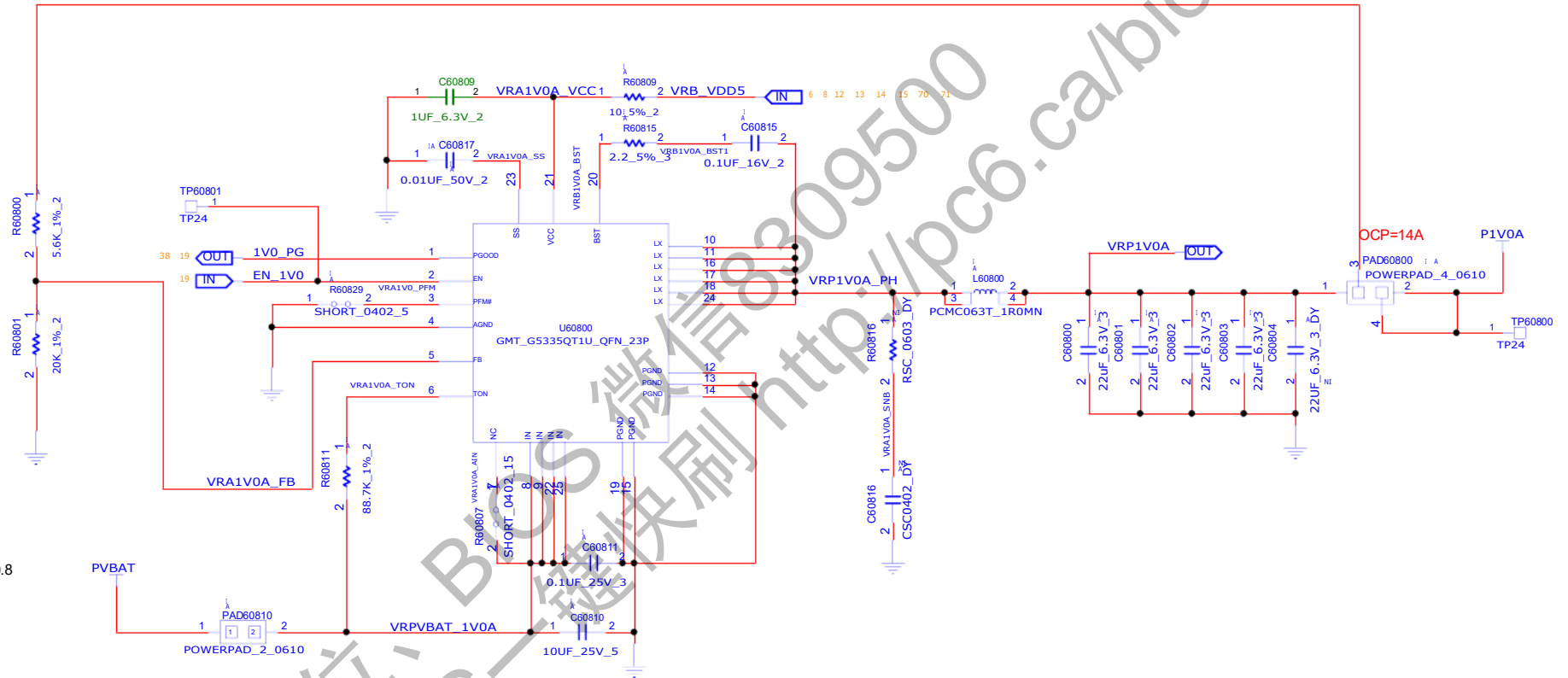
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Throne Block R15 Diagram

SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET		10 of 74	

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PCB P/N	6050A2940901	PCB VER	A01

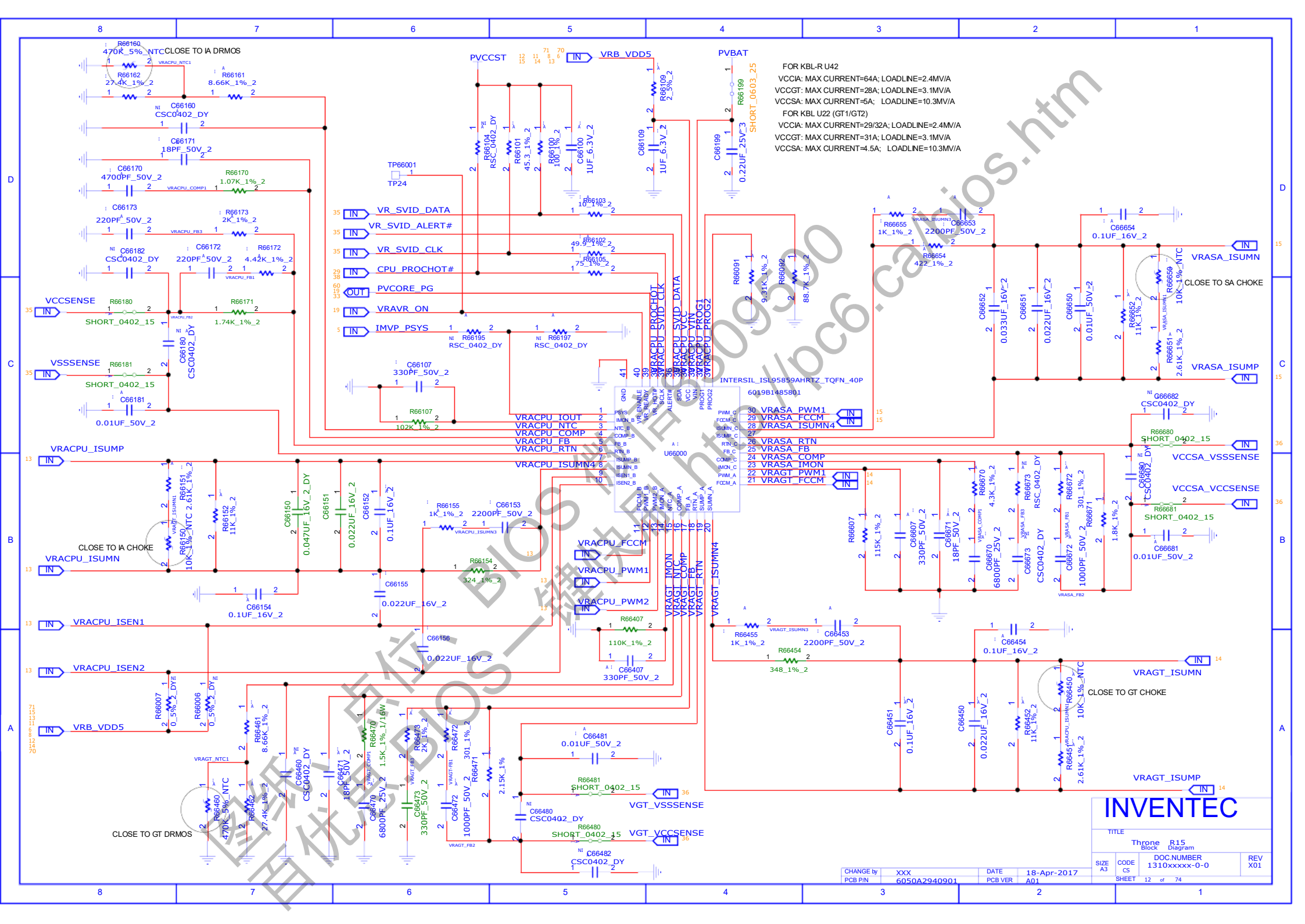
FSW=500KHZ
 $VO = ((R6200/R6201+1)*0.8$



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TITLE			
Throne R15 Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01
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CHANGE by XXX	DATE 18-Apr-2017
PCB P/N 6050A2940901	PCB VER A01



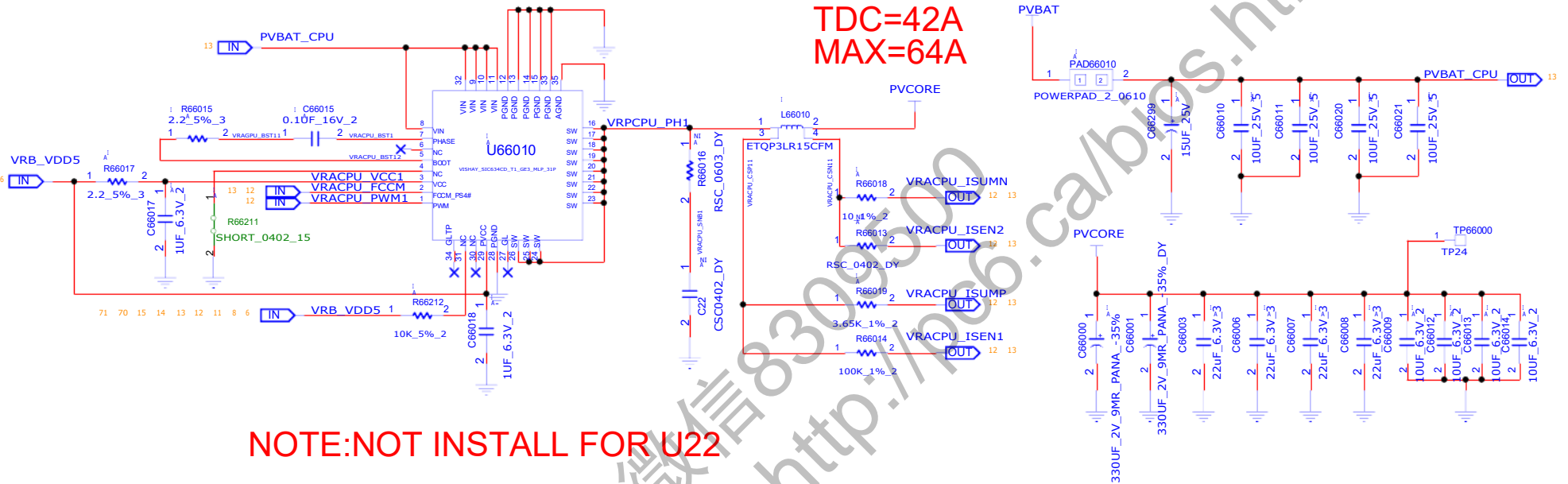
FOR KBL-R U42
VCCA: MAX CURRENT=64A; LOADLINE=2.4MV/A
VCCGT: MAX CURRENT=28A; LOADLINE=3.1MV/A
VCCSA: MAX CURRENT=5A; LOADLINE=10.3MV/A
FOR KBL U22 (GT1/GT2)
VCCA: MAX CURRENT=29/32A; LOADLINE=2.4MV/A
VCCGT: MAX CURRENT=31A; LOADLINE=3.1MV/A
VCCSA: MAX CURRENT=4.5A; LOADLINE=10.3MV/A

TITLE			
Throne R15 Diagram			
SIZE	CODE	DOC NUMBER	
A3	CS	1310xxxx-0-0	
SHEET		12	of 74
REV		X01	

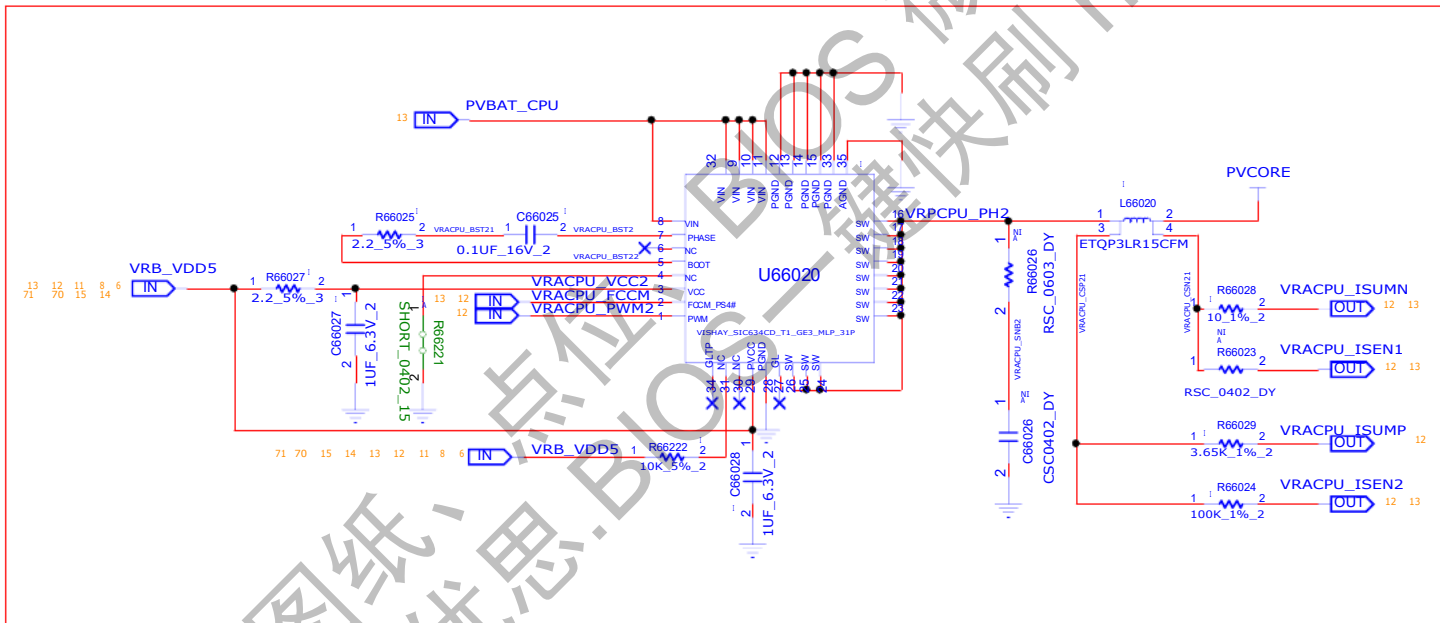
CHANGE by	XXX	DATE	18-Apr-2017
PCB P/N	6050A2940901	PCB VER	A01

NOTE:ONE PHASE FOR U22

TDC=42A
MAX=64A



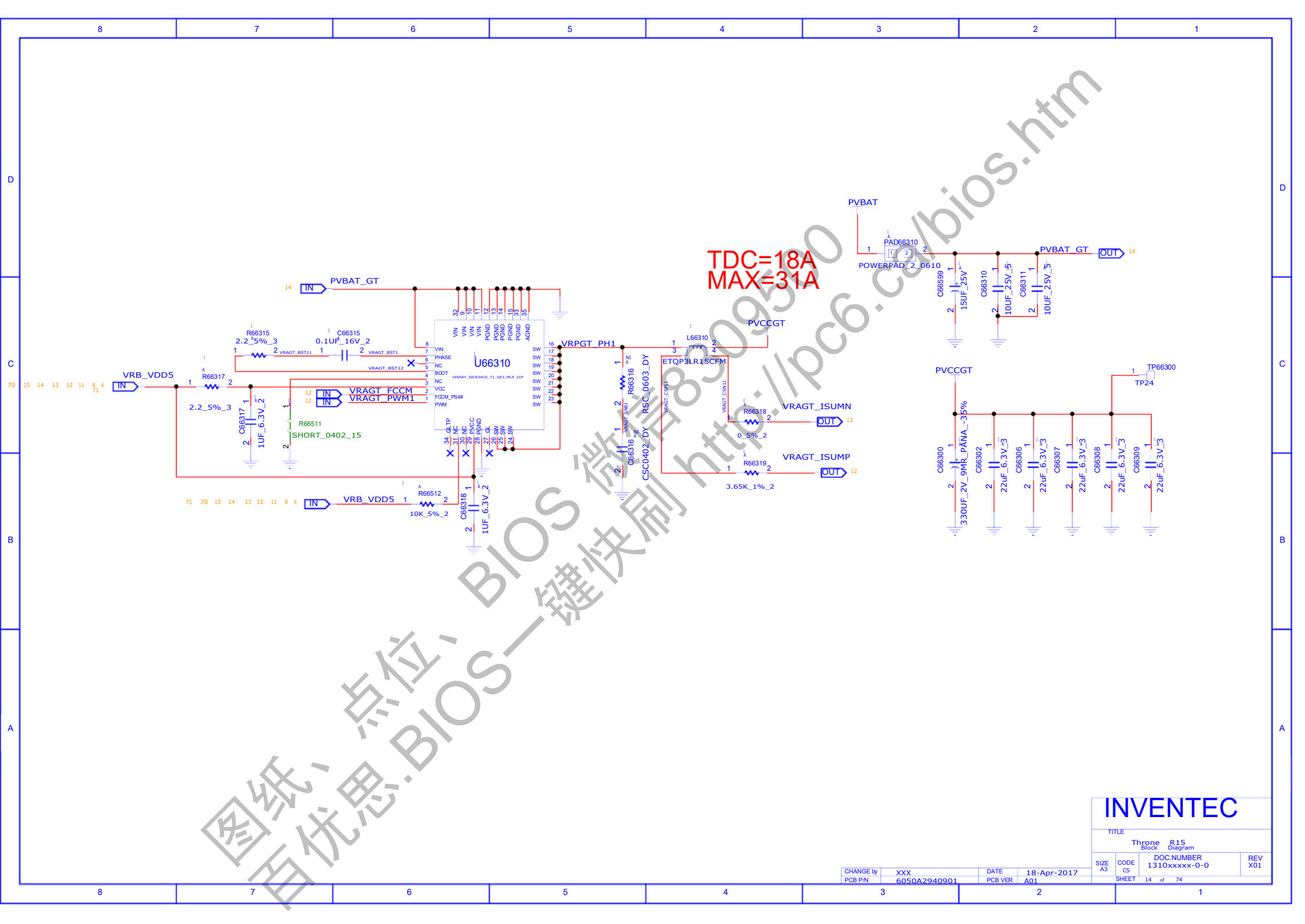
NOTE:NOT INSTALL FOR U22



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TITLE			
Throne R15 Diagram			
DOC NUMBER 1310xxxx-0-0			
SIZE A3	CODE CS	SHEET 13 of 74	REV X01

CHANGE by	XXX	DATE	18-Apr-2017
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TDC=18A
MAX=31A

INVENTEC

TITLE

Throne R15
Diagram

CHANGE by
PCB P/N

XXX
6050A2940901

DATE
PCB VER

18-Apr-2017
A01

SIZE
A3

CODE
CS

DOC NUMBER
1310xxxxx-0-0

REV
X01

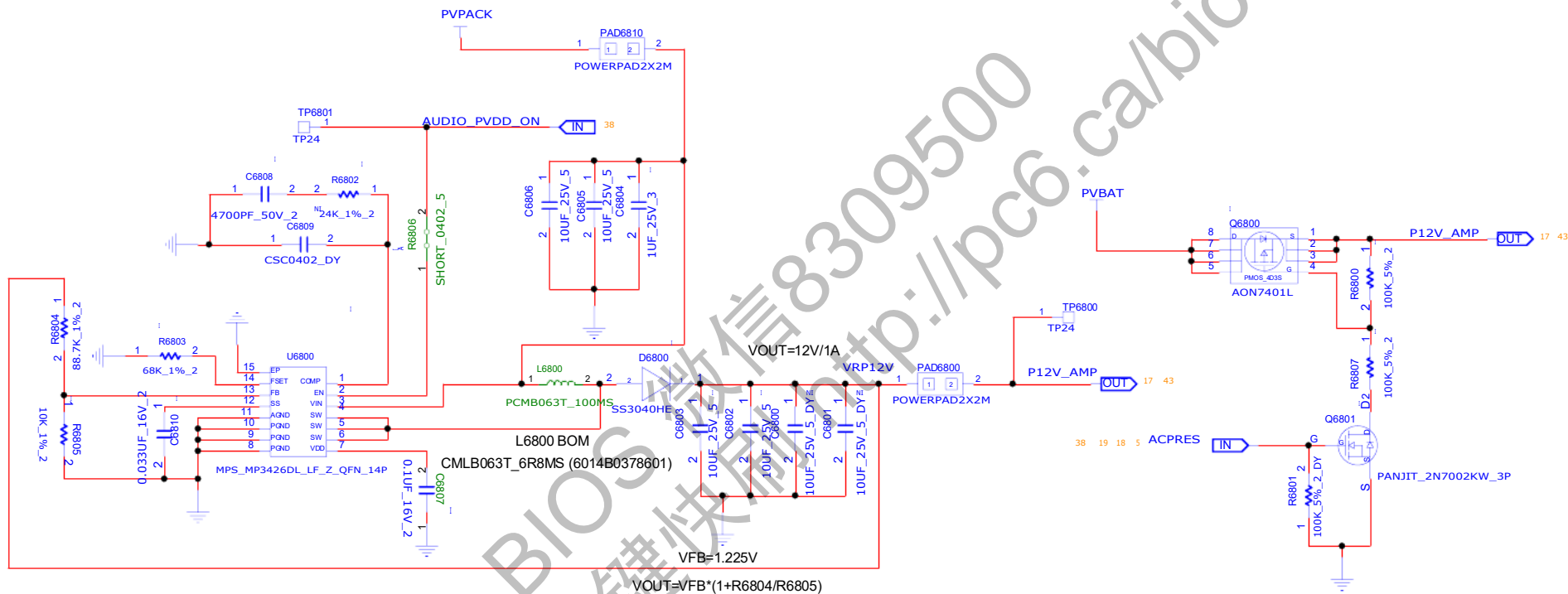
SHEET
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U42			U22		
Location	IEC P/N	Description	Location	IEC P/N	Description
C88150	6010B0046101	CAP-CHIP,0.047UF,16V,K,X7R,0402,TAP	C88150	6010A0000101	CAP-CHIP-223-K,16V-X7R-0402-TAP
C88151	6010B0010101	CHIP,0.033UF,16V,K,X7R,0402,TR	C88151	6010B0010101_DY	CHIP,0.033UF,16V,K,X7R,0402,TR
R88006	60130B0000ZT_DY	RES-CHIP-00HM-5%-1/16W-0402-TAP	R88006	60130B0000ZT	RES-CHIP-00HM-5%-1/16W-0402-TAP
R88007	60130B0000ZT_DY	RES-CHIP-00HM-5%-1/16W-0402-TAP	R88007	60130B0000ZT	RES-CHIP-00HM-5%-1/16W-0402-TAP
C88155	6010A0000101	CAP-CHIP-223-K,16V-X7R-0402-TAP	C88155	6010A0000101_DY	CAP-CHIP-223-K,16V-X7R-0402-TAP
C88156	6010A0000101	CAP-CHIP-223-K,16V-X7R-0402-TAP	C88156	6010A0000101_DY	CAP-CHIP-223-K,16V-X7R-0402-TAP
R88154	6013A008780S	RES-CHIP-383-1%-1/16W-0402-TAP	R88154	6013A008780S	RES-CHIP-287-1%-1/16W-0402-TAP
R88171	6013A0088207	RES-CHIP-3.65K-1%-1/16-0402-TAP	R88171	6013B0097601	RES-CHIP,1.69K,1%,1/16W,0402,TAP
R88107	6013A0088708	RES-CHIP-107K-1%-1/16-0402-TAP	R88107	6013A0014701	RES-CHIP-100K-1%-1/16W-0402-TAP
C88020	6010B0150801	CHIP,10UF,25V,K,X5R,0805,TR,1.25MM	C88020	6010B0150801_DY	CHIP,10UF,25V,K,X5R,0805,TR,1.25MM
C88021	6010B0150801	CHIP,10UF,25V,K,X5R,0805,TR,1.25MM	C88021	6010B0150801_DY	CHIP,10UF,25V,K,X5R,0805,TR,1.25MM
R88014	6013A0014701	RES-CHIP-100K-1%-1/16W-0402-TAP	R88014	6013A0014701_DY	RES-CHIP-100K-1%-1/16W-0402-TAP
U88020	6019B1530201	IC,MOSFET DRIVER,40A,MLP55-31L,31P,TR	U88020	6019B1530201_DY	IC,MOSFET DRIVER,40A,MLP55-31L,31P,TR
L88020	6014B0341701	INDUCTOR,0.15UH,+/- 20%,1MHZ,29A,7.3X8.7X3MM,SMD,TR	L88020	6014B0341701_DY	INDUCTOR,0.15UH,+/- 20%,1MHZ,29A,7.3X8.7X3MM,SMD,TR
R88025	60130B2R200T	RES-CHIP-2.2-5%-1/10W-0803-TAP	R88025	60130B2R200T_DY	RES-CHIP-2.2-5%-1/10W-0803-TAP
C88025	6010A0036403	CHIP,0.1UF,16V,K,X7R,0402,TAP	C88025	6010A0036403_DY	CHIP,0.1UF,16V,K,X7R,0402,TAP
R88027	60130B2R200T	RES-CHIP-2.2-5%-1/10W-0803-TAP	R88027	60130B2R200T_DY	RES-CHIP-2.2-5%-1/10W-0803-TAP
C88027	6010B0392101	CAPACITOR-CHIP,1UF,6.3V,K,X5R,0402,TR	C88027	6010B0392101_DY	CAPACITOR-CHIP,1UF,6.3V,K,X5R,0402,TR
C88028	6010B0392101	CAPACITOR-CHIP,1UF,6.3V,K,X5R,0402,TR	C88028	6010B0392101_DY	CAPACITOR-CHIP,1UF,6.3V,K,X5R,0402,TR
R88024	6013A0014701	RES-CHIP-100K-1%-1/16W-0402-TAP	R88024	6013A0014701_DY	RES-CHIP-100K-1%-1/16W-0402-TAP
R88028	6013A0014201	RES-CHIP-100HM-1%-1/16W-0402-TAP	R88028	6013A0014201_DY	RES-CHIP-100HM-1%-1/16W-0402-TAP
R88029	6013A0088207	RES-CHIP-3.65K-1%-1/16-0402-TAP	R88029	6013A0088207_DY	RES-CHIP-3.65K-1%-1/16-0402-TAP
R88222	60130B1030ZT	CHIP,10K,5%,1/16W,0402,TR	R88222	60130B1030ZT_DY	CHIP,10K,5%,1/16W,0402,TR
C88000	6010B0136301	CAPACITOR-AL-SP,330UF,2V,-35%/+10%,105C,DX1.9,SMD,TR,9MOHM	C88000	6010B0219101	SP,220UF,2V,M,105C,DX1.9,SMD,TR,6MOHM

INVENTEC

TITLE			
Throne R15 Block Diagram			
SIZE A3		CODE CS	DOC NUMBER 1310xxxx-0-0
SHEET 16 of 74		REV X01	

CHANGE by	XXX	DATE	18-Apr-2017
PCB P/N	6050A2940901	PCB VER	A01

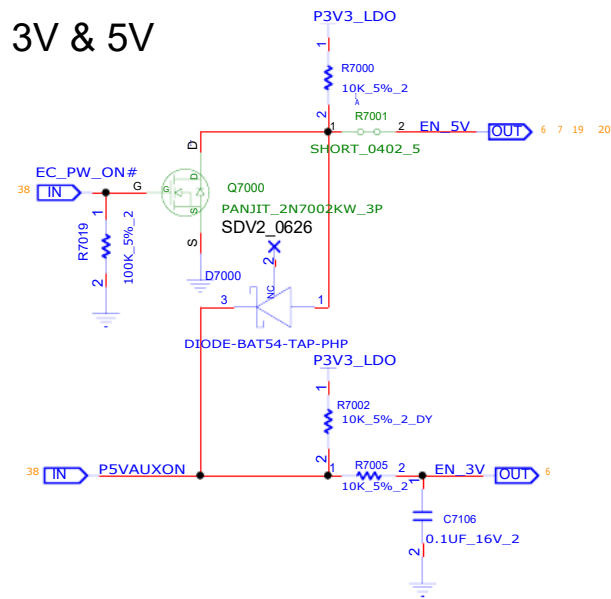


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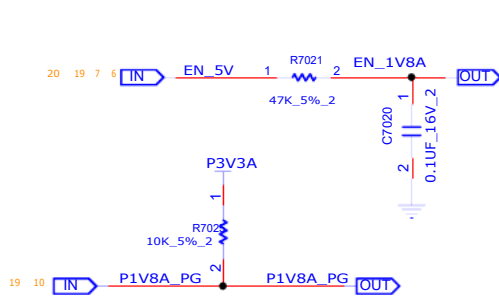
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Throne R15 Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET 17	of 74		

CHANGE by XXX	DATE 18-Apr-2017
PCB P/N 6050A2940901	PCB VER A01

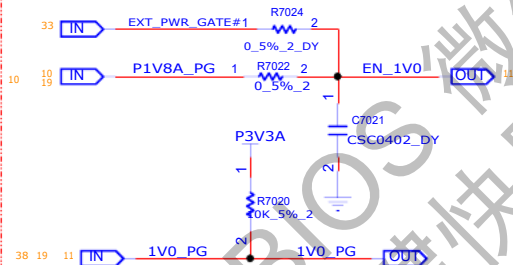
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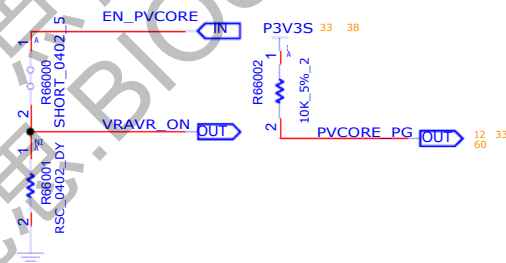
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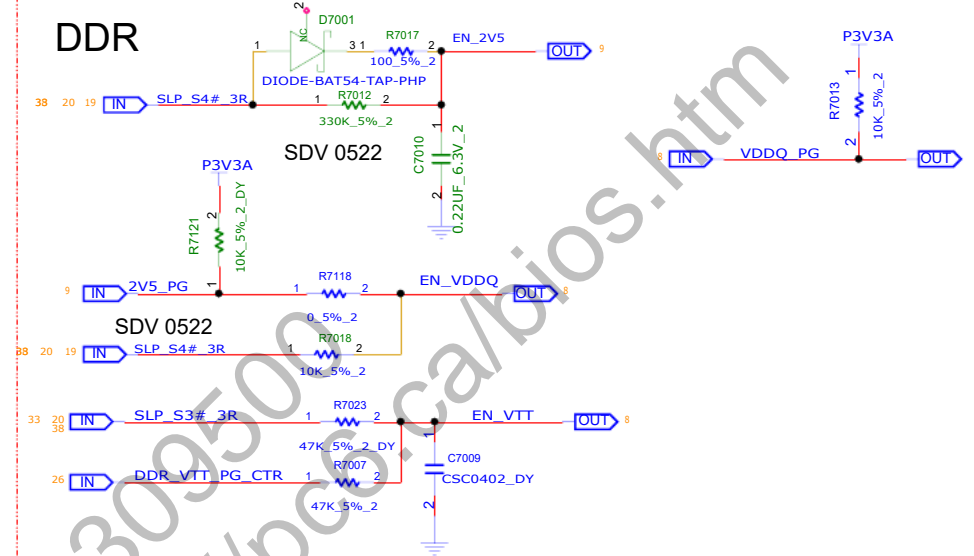
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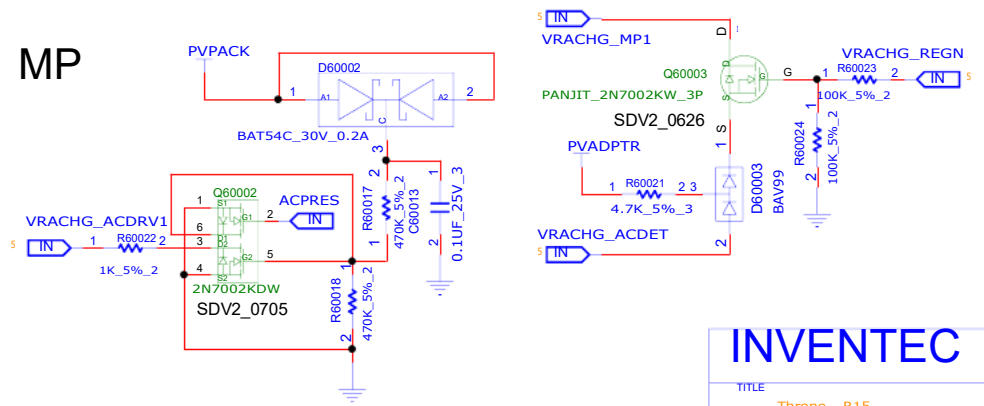
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DDR



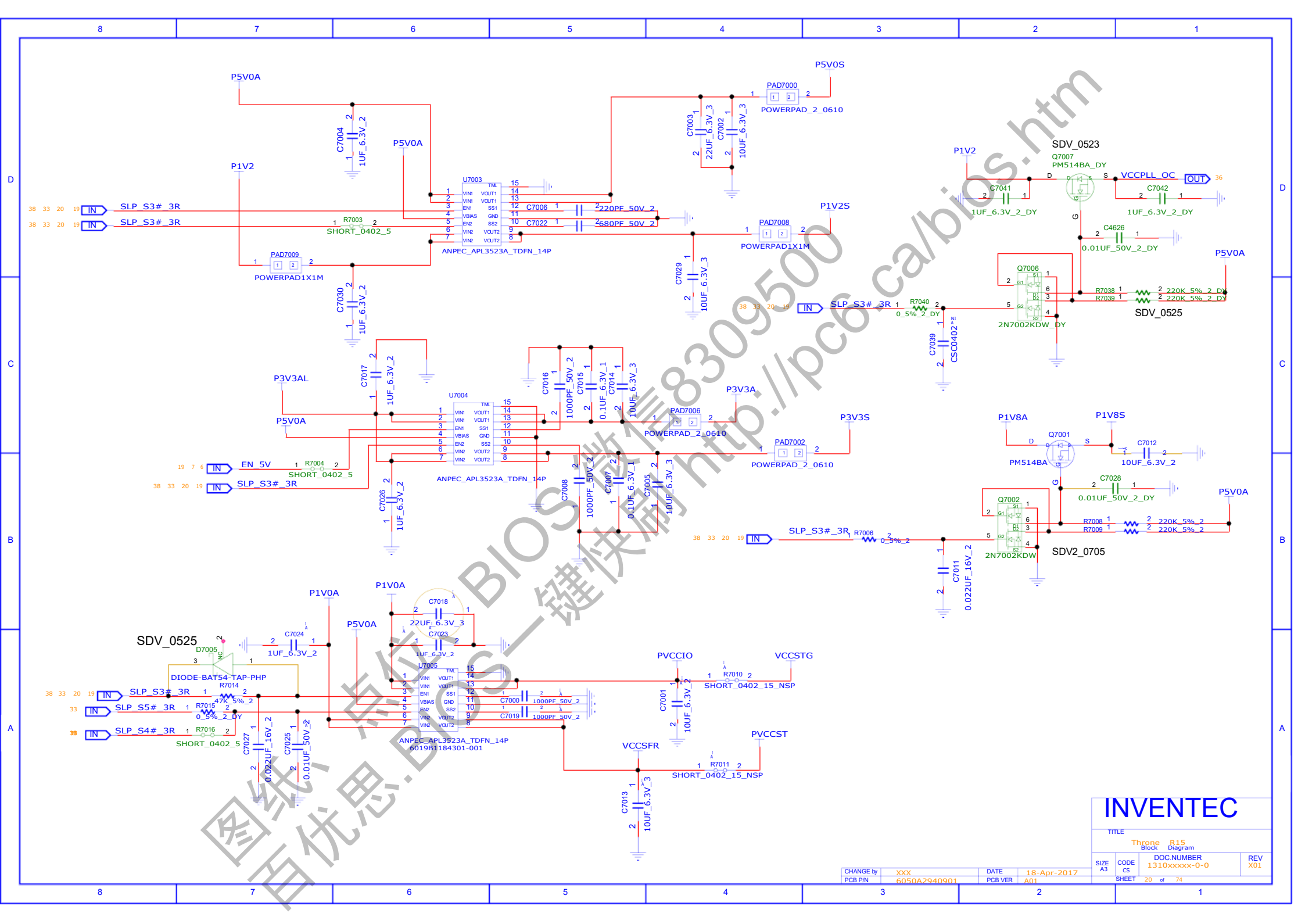
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CHANGE by	XXX	DATE	18-Apr-2017
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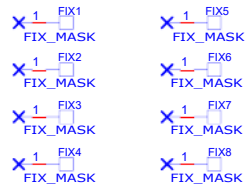
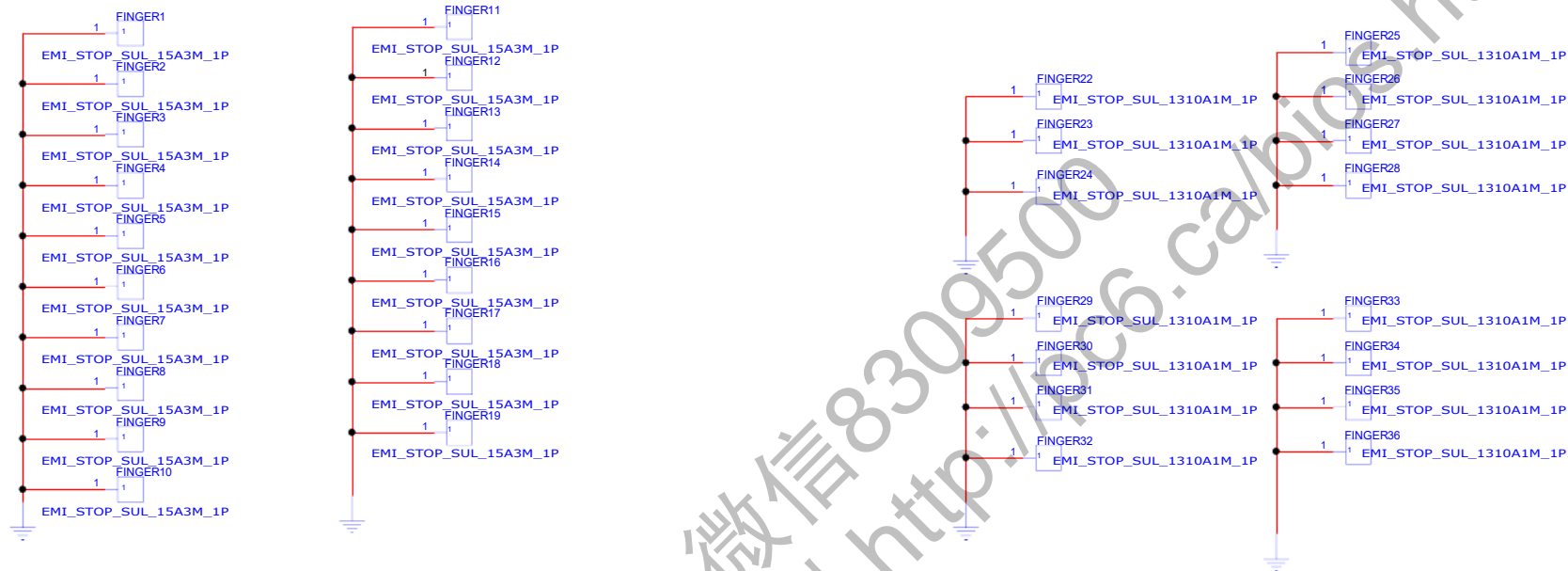


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Throne R15 Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01
SHEET 20	of 74		

CHANGE by XXX	DATE 18-Apr-2017
PCB P/N 6050A2940901	PCB VER A01

REFERENCE 0~49(PCB SCREW)

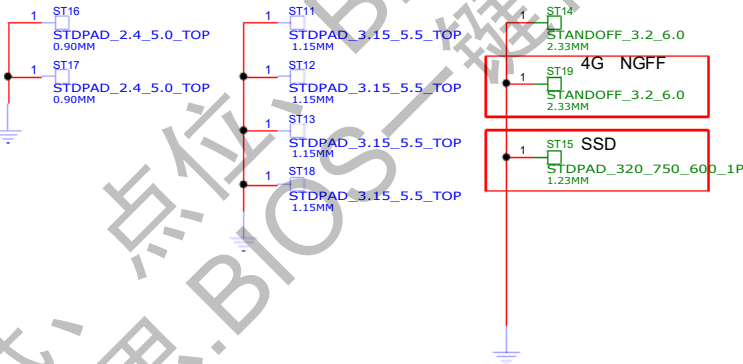


GPU

FAN

CPU

PCB



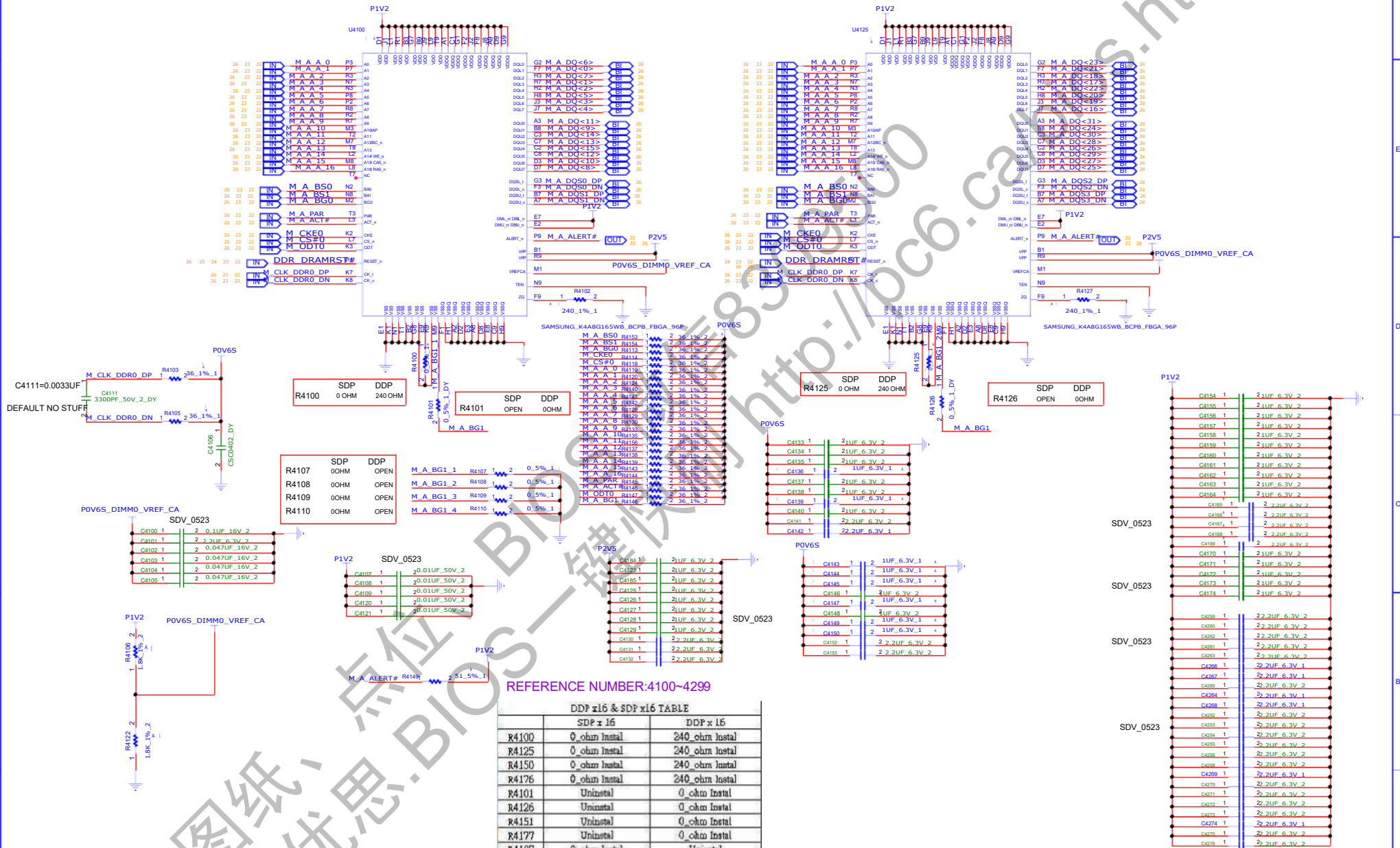
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SHEET 21 of 74			

CHANGE by	XXX	DATE	18-Apr-2017
PCB P/N	6050A2940901	PCB VER	A01

F
E
D
C
B
A

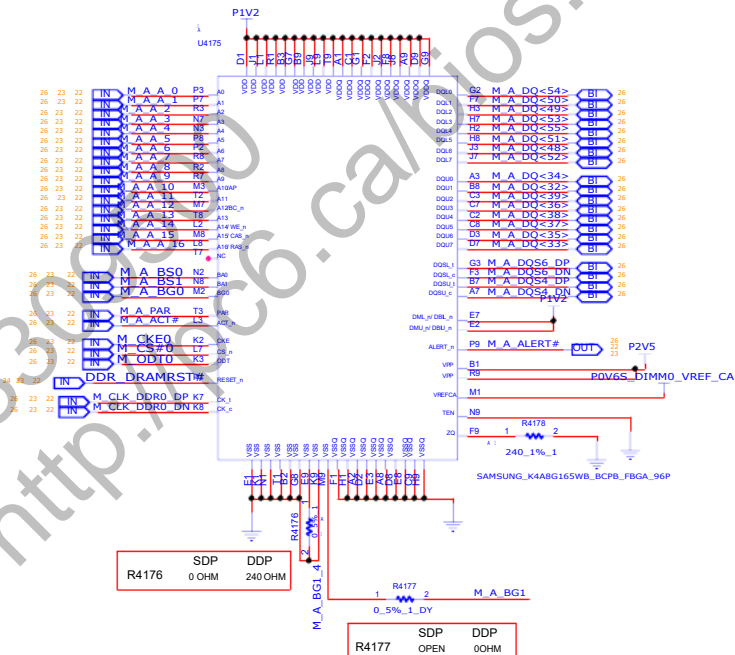
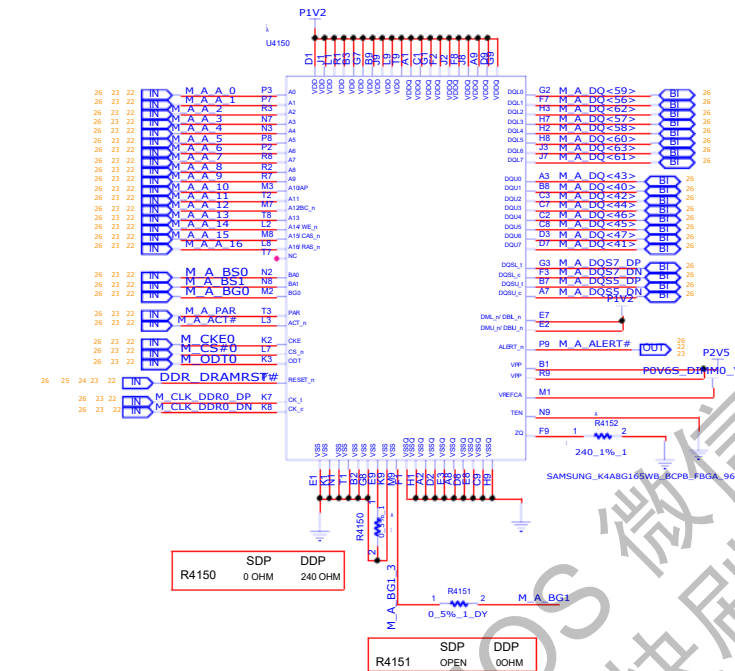
F
E
D
C
B
A



REFERENCE NUMBER:4100-4299

DDP x16 & SDP x16 TABLE		
	SDP x 16	DDP x 16
R4100	0 ohm instal	240 ohm instal
R4125	0 ohm instal	240 ohm instal
R4150	0 ohm instal	240 ohm instal
R4176	0 ohm instal	240 ohm instal
R4101	Uninstal	0 ohm instal
R4126	Uninstal	0 ohm instal
R4151	Uninstal	0 ohm instal
R4177	Uninstal	0 ohm instal
R4107	0 ohm instal	Uninstal
R4108	0 ohm instal	Uninstal
R4109	0 ohm instal	Uninstal
R4110	0 ohm instal	Uninstal

INVENTEC



DDF x16 & SDF x16 TABLE		
	SDF x16	DDF x16
R4100	0_ohm Instal	240_ohm Instal
R4125	0_ohm Instal	240_ohm Instal
R4150	0_ohm Instal	240_ohm Instal
R4176	0_ohm Instal	240_ohm Instal
R4101	Uninstal	0_ohm Instal
R4126	Uninstal	0_ohm Instal
R4151	Uninstal	0_ohm Instal
R4177	Uninstal	0_ohm Instal
R4107	0_ohm Instal	Uninstal
R4108	0_ohm Instal	Uninstal
R4109	0_ohm Instal	Uninstal
R4110	0_ohm Instal	Uninstal

REFERENCE NUMBER:4100~4299

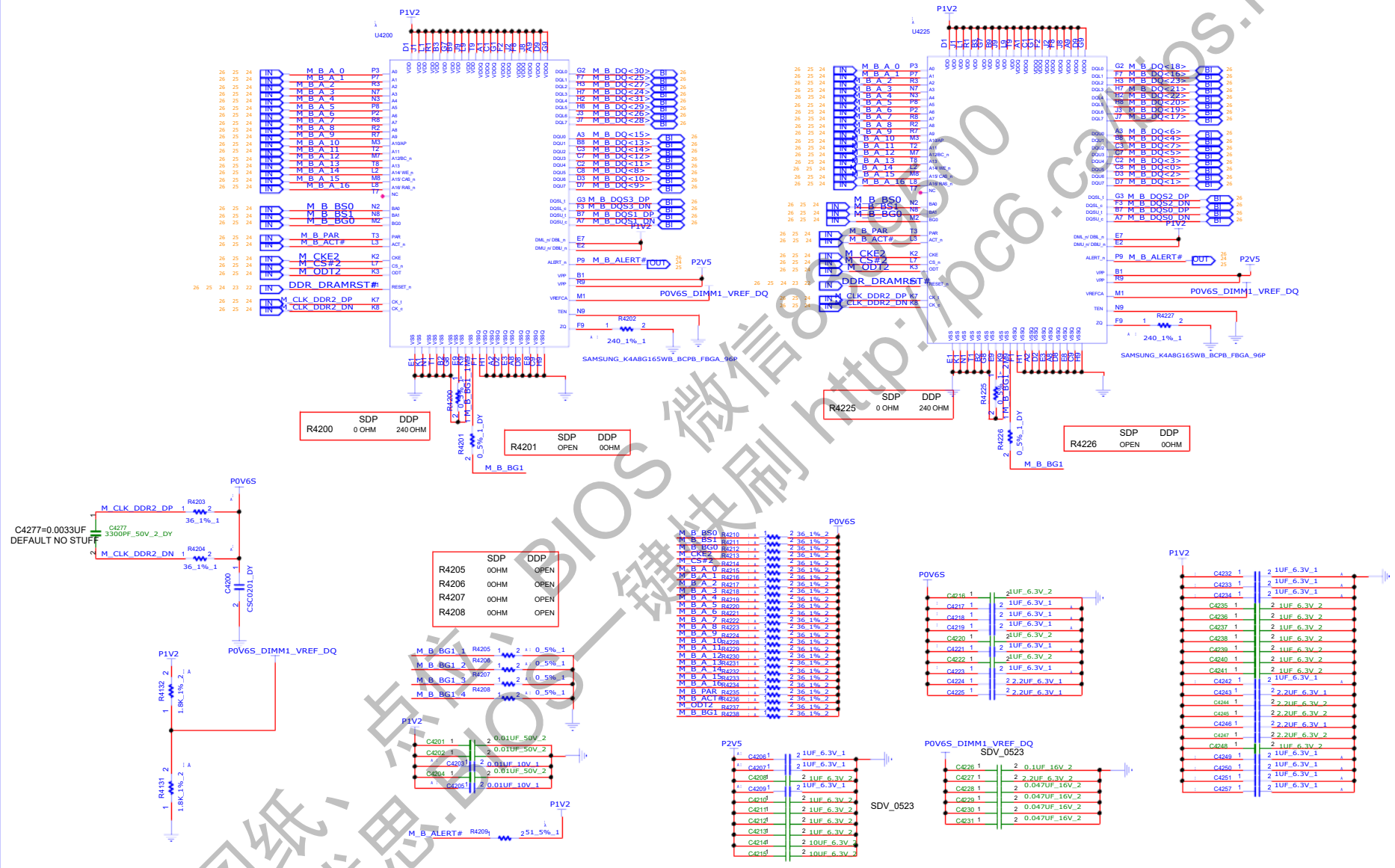
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TITLE		Throne R15	
Block		Diagram	
SIZE	CODE	DOCNUMBER	REV
A3	C5	131Dxxxxx-0-0	X01
SHEET		23	of 26

CHANGE BY	DATE	PCB VER
XXX	18-Apr-2017	A01
PCB PIN	PCB VER	
6050A2940901		

F
E
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A

F
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A

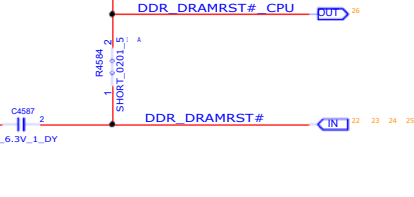
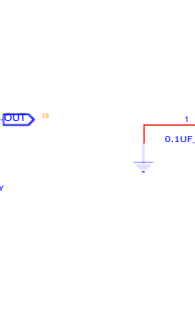
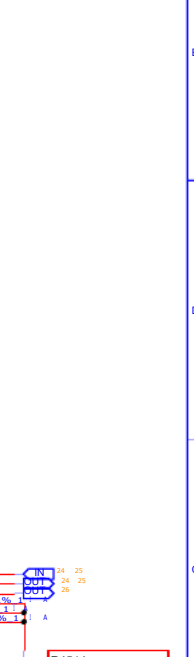
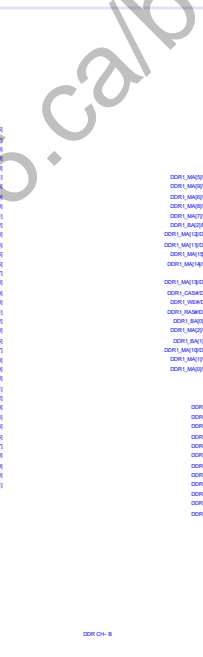


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Block: Diagram			
SIZE: A3	CODE: CS	DOCNUMBER: 131Dxxxx-0-0	REV: X01
CHANGE BY: XXX		DATE: 18-Apr-2017	REV: X01
PCB PIN: C050A2940901		PCB VER: A01	
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INVENTEC

TITLE			
Throne		R15	
Block		Diagram	
SIZE A3	CODE CS	DOCNUMBER 1310xxxxx-0-0	REV X01
SHEET		25	of 74

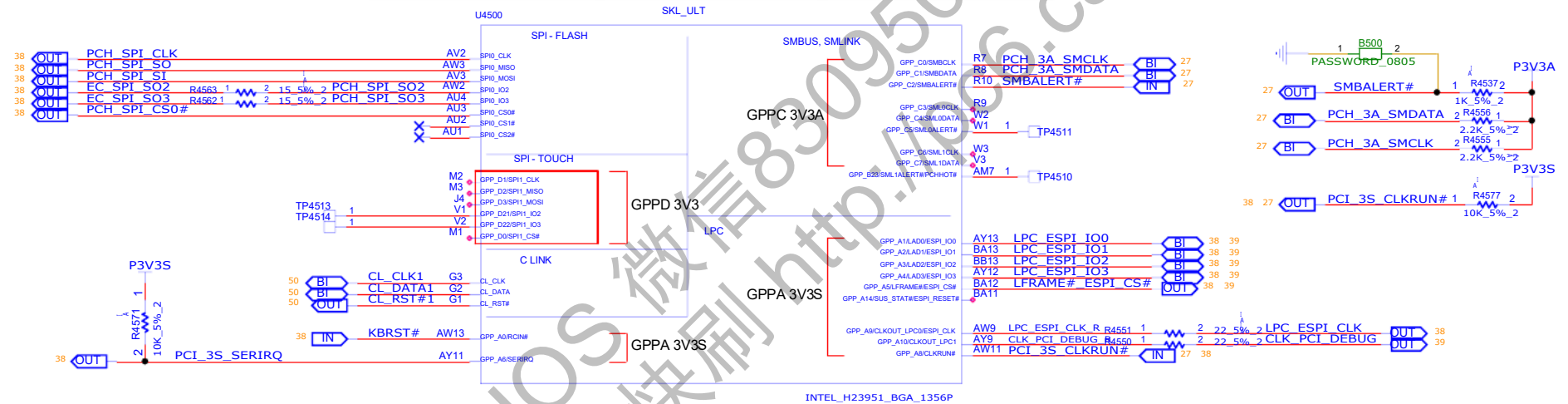


543016 60.3.31: ALL UNUSED GPIOs (WHICH DEFAULT TO GPIO FUNCTIONALITY) DO NOT NEED TERMINATION

All GPIOs have weak internal pull-up/pull-down resistors which are off by default. The Internal PU/PD can be programmed (PU/PD/None) by BIOS after reset.

GPIO Group Summary

GPIO Group	Power Pins	Voltage
Primary Well Group A (GPP_A)	VCCPGPPA	1.8V or 3.3V
Primary Well Group B (GPP_B)	VCCPGPPB	1.8V or 3.3V
Primary Well Group C (GPP_C)	VCCPGPPC	1.8V or 3.3V
Primary Well Group D (GPP_D)	VCCPGPPD	1.8V or 3.3V
Primary Well Group E (GPP_E)	VCCPGPPE	1.8V or 3.3V
Primary Well Group F (GPP_F)	VCCPGPPF	1.8V
Primary Well Group G (GPP_G)	VCCPGPPG	1.8V or 3.3V
Deep Sleep Well Group (GPD)	VCCPD9W_3p3	3.3V



INVENTEC

TITLE
Throne R15
Diagram

SIZE A3
CODE CS
SHEET 27 of 74

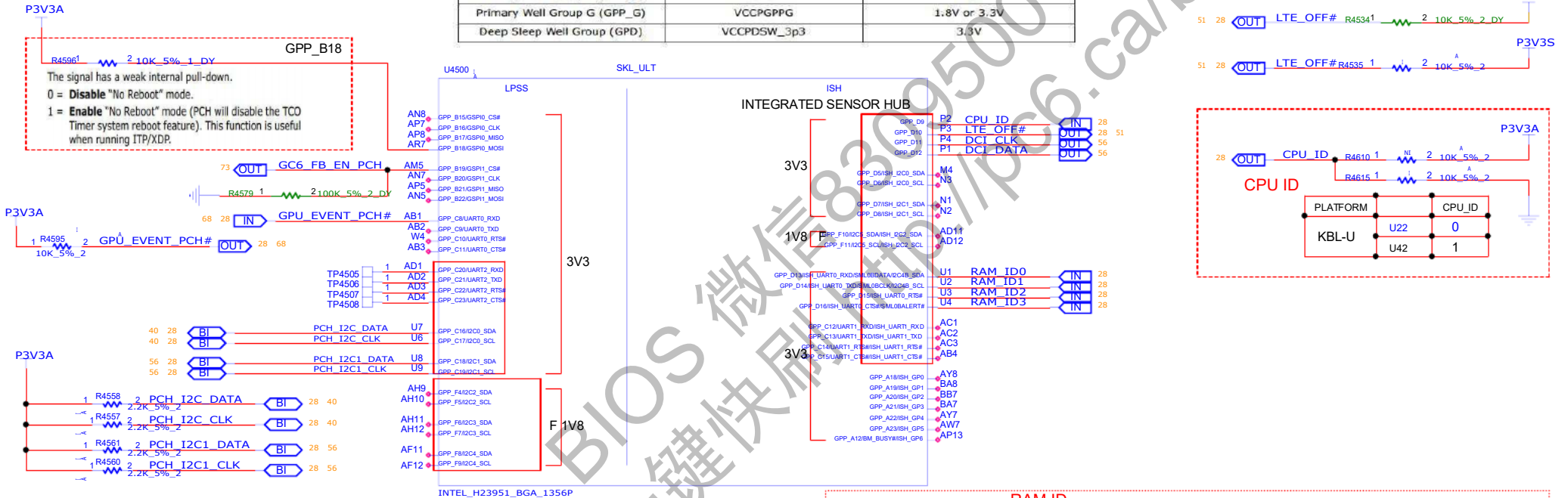
CHANGE by XENG>
PCB P/N 6050A2940901
DATE 18-Apr-2017
PCB VER A0VER>

DOC NUMBER
1310xxxxx-0-0
REV X01

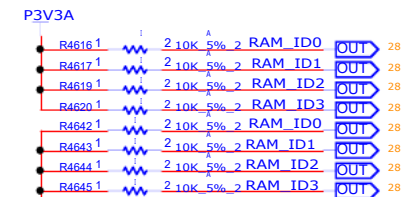
All GPIOs have weak internal pull-up/pull-down resistors which are off by default. The internal PU/PD can be programmed (PU/PD/None) by BIOS after reset.

GPIO Group Summary

GPIO Group	Power Pins	Voltage
Primary Well Group A (GPP_A)	VCCPGPPA	1.8V or 3.3V
Primary Well Group B (GPP_B)	VCCPGPPB	1.8V or 3.3V
Primary Well Group C (GPP_C)	VCCPGPPC	1.8V or 3.3V
Primary Well Group D (GPP_D)	VCCPGPPD	1.8V or 3.3V
Primary Well Group E (GPP_E)	VCCPGPPE	1.8V or 3.3V
Primary Well Group F (GPP_F)	VCCPGPPF	1.8V
Primary Well Group G (GPP_G)	VCCPGPPG	1.8V or 3.3V
Deep Sleep Well Group (GPD)	VCCPDSW_3p3	3.3V



	RAM_ID3	RAM_ID2	RAM_ID1	RAM_ID0
DIMM	0	0	0	0
SAMSUNG 4G	0	0	0	1
SAMSUNG 8G	0	0	1	0
SAMSUNG 16G	0	0	1	1
HYNIX 4G	0	1	0	0
HYNIX 8G	0	1	0	1
HYNIX 16G	0	1	1	0
MICRO 4G	0	1	1	1
MICRO 8G	1	0	0	0
MICRO 16G	1	0	0	1

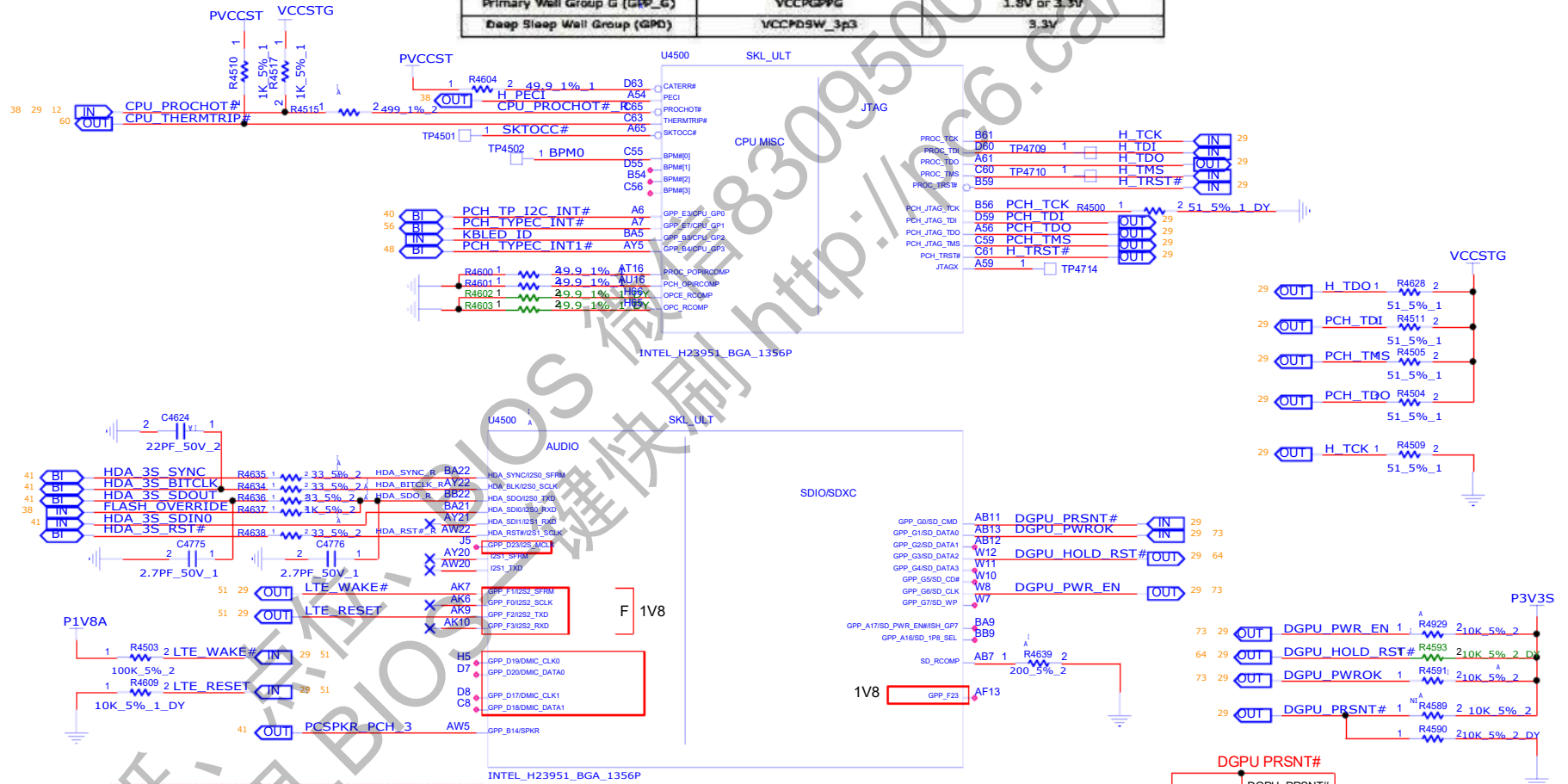


INVENTEC

TITLE			
Throne R15 Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01
SHEET 28 of 74			

All GPIOs have weak internal pull-up/pull-down resistors which are off by default. The internal PU/PD can be programmed (PU/PD/None) by BIOS after reset.

GPIO Group	Power Pins	Voltage
Primary Well Group A (GPP_A)	VCCPGPPA	1.8V or 3.3V
Primary Well Group B (GPP_B)	VCCPGPPB	1.8V or 3.3V
Primary Well Group C (GPP_C)	VCCPGPPC	1.8V or 3.3V
Primary Well Group D (GPP_D)	VCCPGPPD	1.8V or 3.3V
Primary Well Group E (GPP_E)	VCCPGPPE	1.8V or 3.3V
Primary Well Group F (GPP_F)	VCCPGPPF	1.8V
Primary Well Group G (GPP_G)	VCCPGPPG	1.8V or 3.3V
Deep Sleep Well Group (GPD)	VCCPDW_3p3	3.3V



DGPU PRSNT#	
	DGPU_PRSNT#
DIS	0
UMA	1

INVENTEC

TITLE			
Throne Block R15 Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET 29 of 74			

CHANGE by	XENG>	DATE	18-Apr-2017
PCB P/N	6050A2940901	PCB VER	A0VER>

Table 24-3. PCI Express® Link Configurations Supported

SKL	PCIe Link Config	PCI Express® Lanes											
		1	2	3	4	5	6	7	8	9	10	11	12
U	1x4	Port1				Port5				Port9			
	2x2	Port1	Port3	Port5	Port7	Port9	Port11	Port12					
	1x2 + 2x1	Port1	Port3	Port4	Port5	Port7	Port8	Port9	Port11	Port12			
	4x1	Port1	Port2	Port3	Port4	Port5	Port6	Port7	Port8	Port9	Port10	Port11	Port12
Y	1x4	Port1				Port5				Port9			
	2x2	Port1	Port3	Port5	Port7	Port9	Port11	Port12					
	1x2 + 2x1	Port1	Port3	Port4	Port5	Port7	Port8	Port9	Port11	Port12			
	4x1	Port1	Port2	Port3	Port4	Port5	Port6	Port7	Port8	Port9	Port10	Port11	Port12
	1x2									Port9			
	2x1									Port9	Port10		

Notes:

1. A PCIe Lane is composed of a single pair of Rx and Tx signals (such as, Rx3+/Rx3- and Tx3+/Tx3- make up PCIe Lane 3). A PCIe Link is composed of one or more PCIe Lanes (such as bundling 2 PCIe Lanes together would make a x2 PCIe Link). A PCIe Link is addressed by the lowest number PCIe Port it connects to in the PCH (such as a x2 PCIe Link connected to PCIe Ports 3 and 4 would be called x2 PCIe Port 3).

Figure 12-4. PCIe_RCOMP and PCIe_RCOMPN Connections

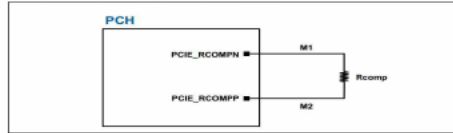


Table 12-9. PCI Express® Compensation Routing Guidelines

Signal	Trace Width	Isolation Spacing	Resistor Value	Max Length	Length Matching
PCIe_RCOMP	M1: 4 mils min (breakout) 12-15 mils (trace) Note: Must maintain low DC resistance routing (<0.1 ohm).	At least 12 mils to any adjacent high speed I/O.	100 ohm +/-1% external resistor. Difference between RCOMP and RCOMPN.	NA	Both RCOMP and RCOMPN need to be matched to less than 1% trace and board.
PCIe_RCOMPN	M2: 4 mils min (breakout) 12-15 mils (trace) Note: Must maintain low DC resistance routing (<0.1 ohm).			NA	

GPU

WLAN

LTE

SSD 2X

SSD 4X

U4500

SKL_ULT

PCIEUSB3/SATA

SSIC/USB3

USB2

TYPE C PORT R2

USB3.0 PORT L1

USB3.0 PORT L2

TYPE-C W/PD PORT R1

USB2.0 TYPE C R2

LTE PORT

USB2.0 PORT L1

USB2.0 TYPE-C_R1

BLUETOOTH

HD WEBCAM

CARDREADER

FINGERPRINT

USB2.0 PORT L2

INVENTEC

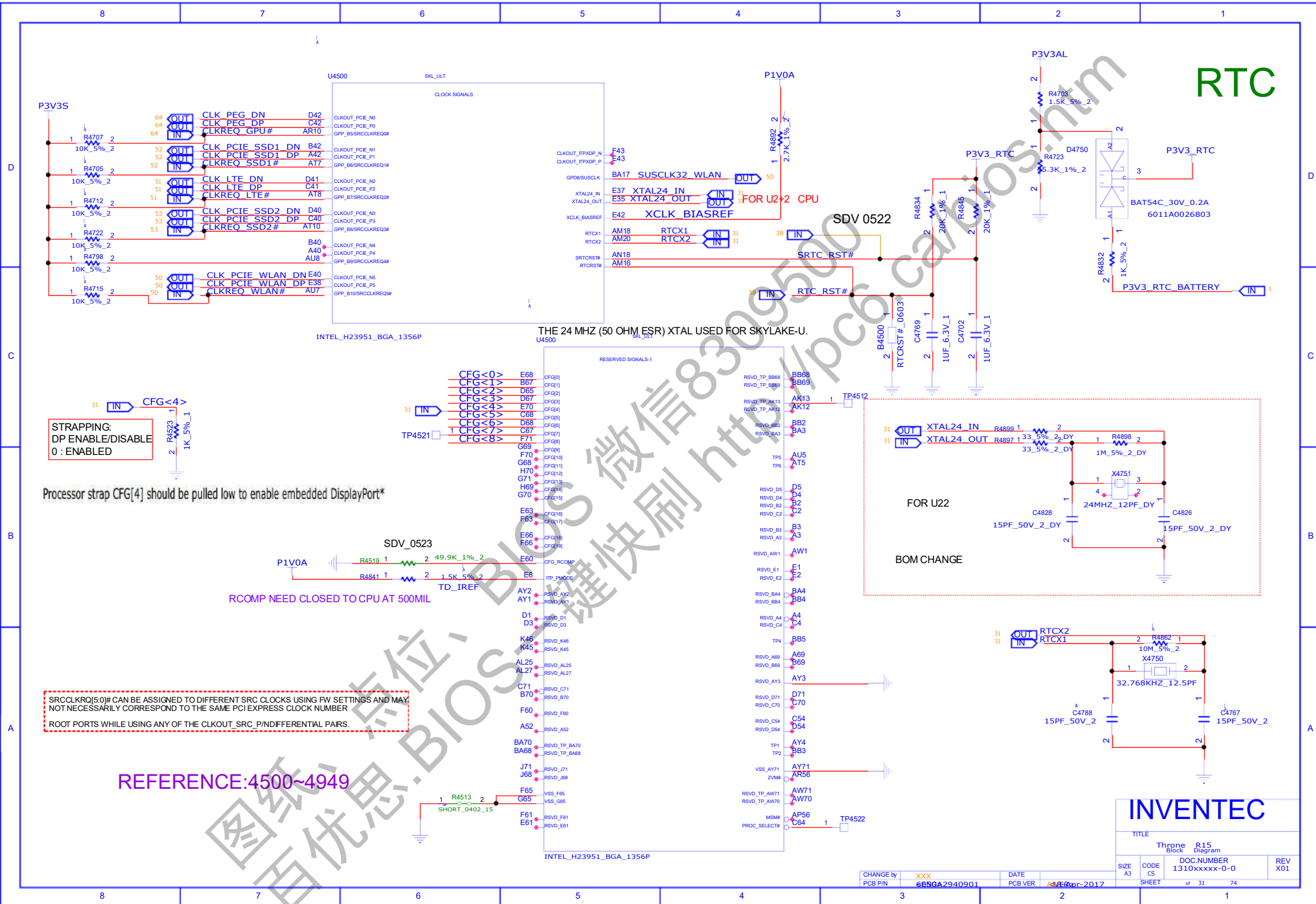
Throne R15 Block Diagram

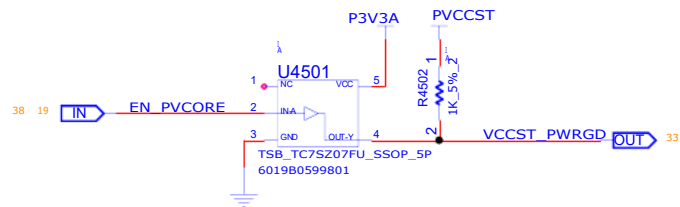
DOCNUMBER 1310xxxxx-0-0

REV X01

CHANGE BY XING> 6050A2940901 DATE 18-Apr-2017 PCB VER A000>

SHEET 30 of 74

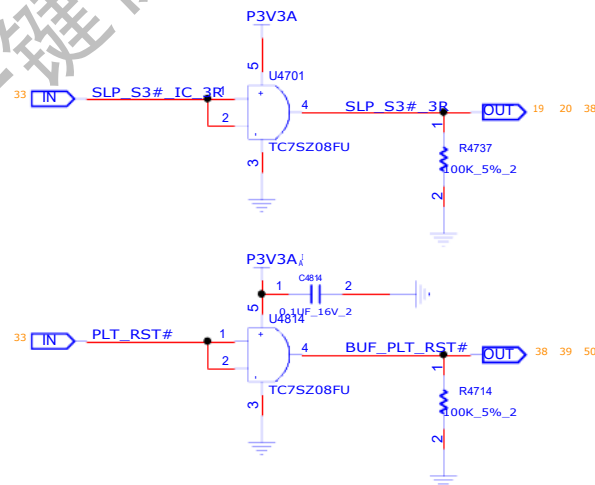
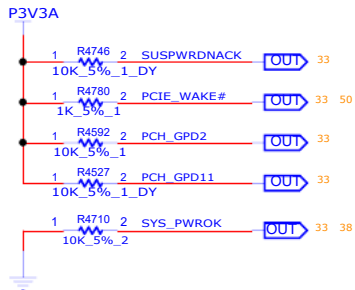
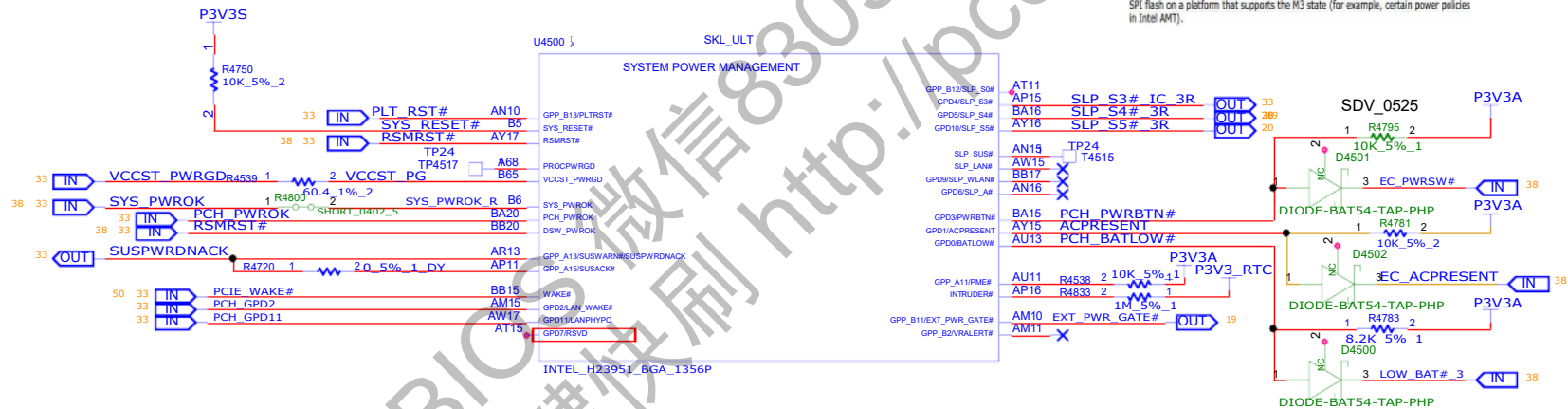




PCH Power OK: When asserted, PCH_PWROK is an indication to the PCH that all of its core power rails have been stable for at least 5 ms. PCH_PWROK can be driven asynchronously. When PCH_PWROK is negated, the PCH asserts PLTRST#.

Note: PCH_PWROK must not glitch, even if RSMRST# is low.

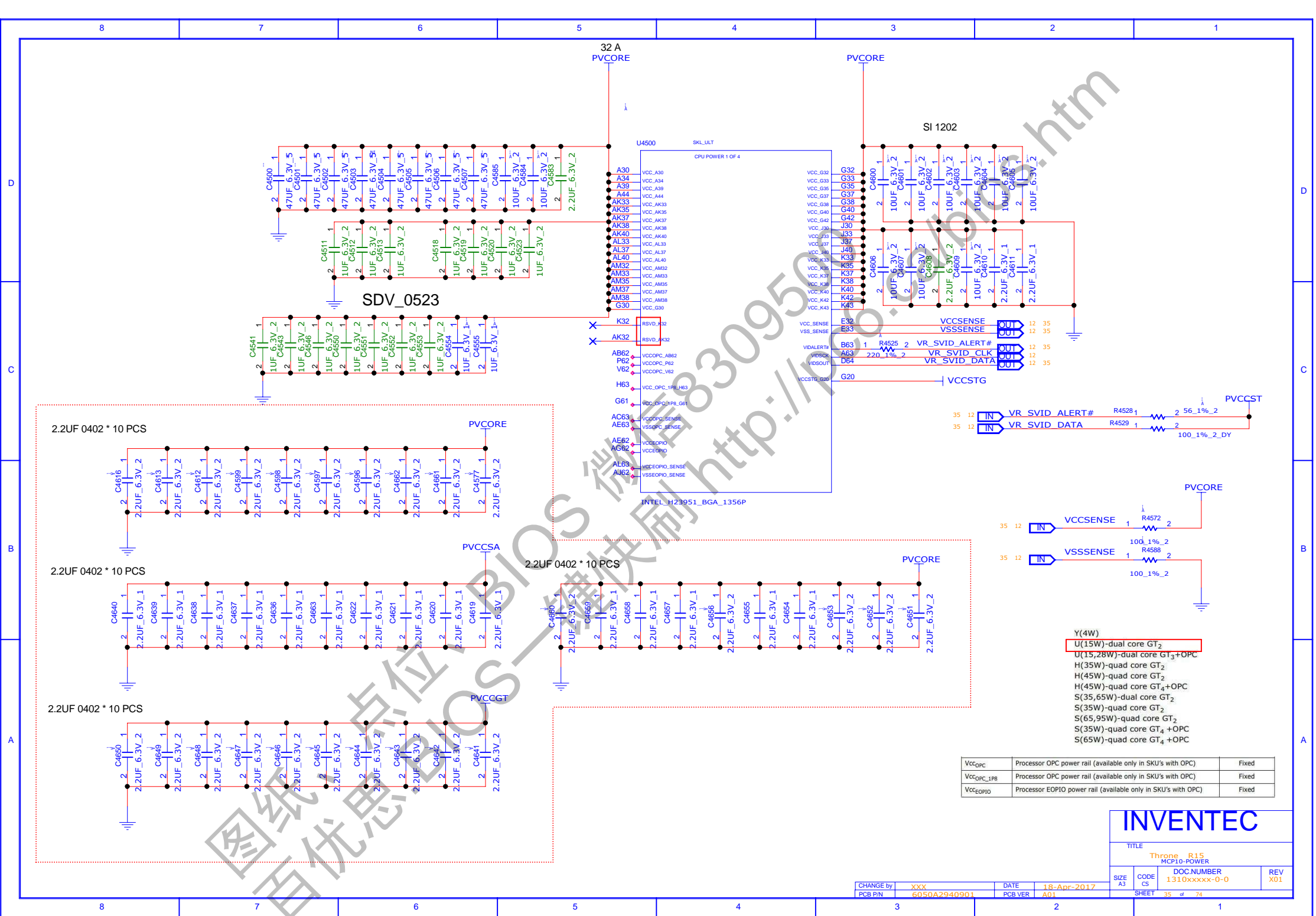
SLP_S# output signal can be used to cut power to the Intel Management Engine and SPI flash on a platform that supports the M3 state (for example, certain power policies in Intel AMT).



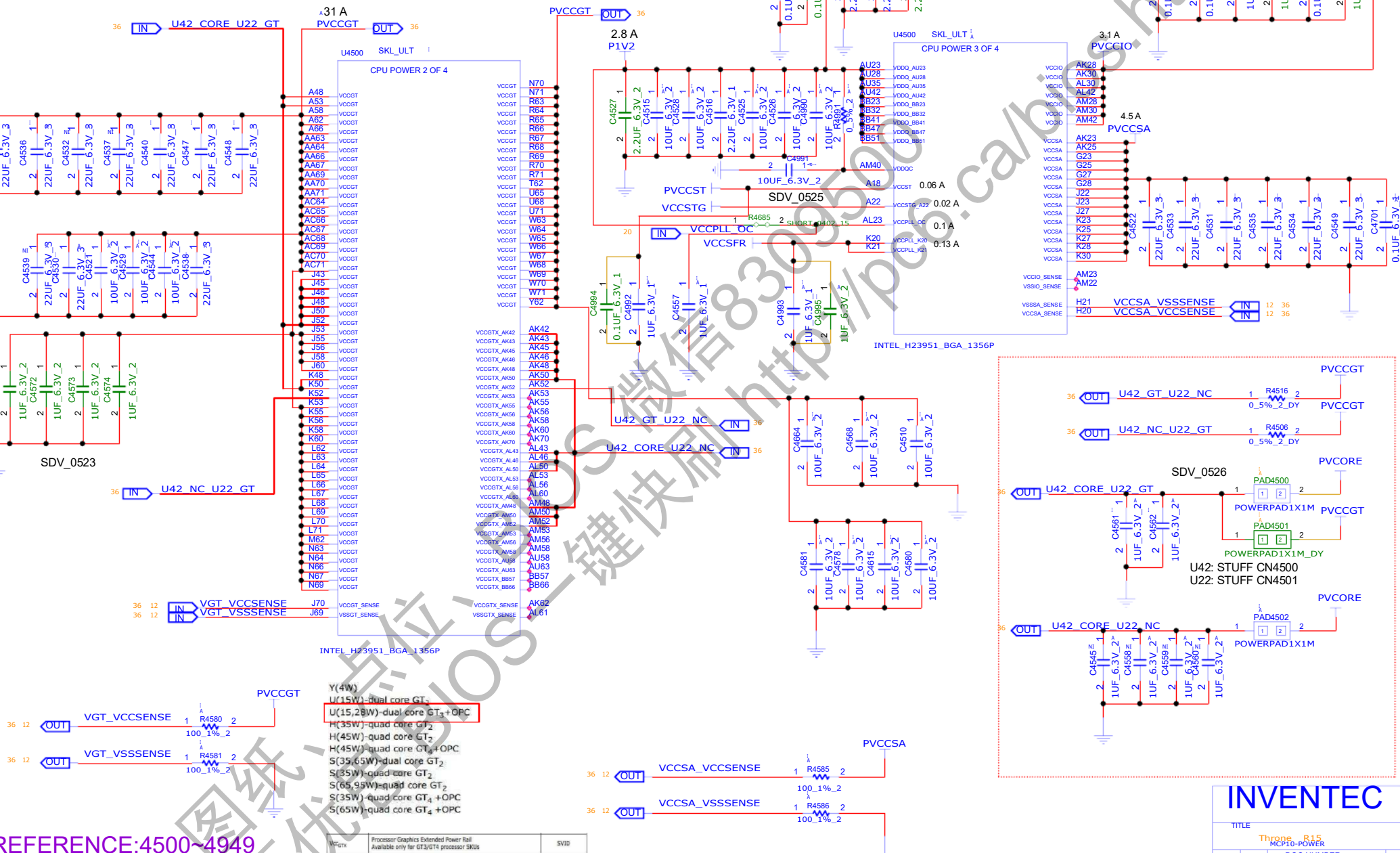
INVENTEC

TITLE			
Throne R15 Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01
SHEET		33 of 74	

CHANGE by	XENG>	DATE	18-Apr-2017
PCB P/N	6050A2940901	PCB VER	AVR>



8	7	6	5	4	3	2	1
---	---	---	---	---	---	---	---



REFERENCE:4500~4949

V _{CC} GTx	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
---------------------	---	------

CHANGE by	XXX	DATE	18-Apr-2017	SIZE	A3	CS	1310xxxxx-U-0	X01
PCB P/N	6050A2940901	PCB VER	A01	SHEET	36	of	74	

D

C

B

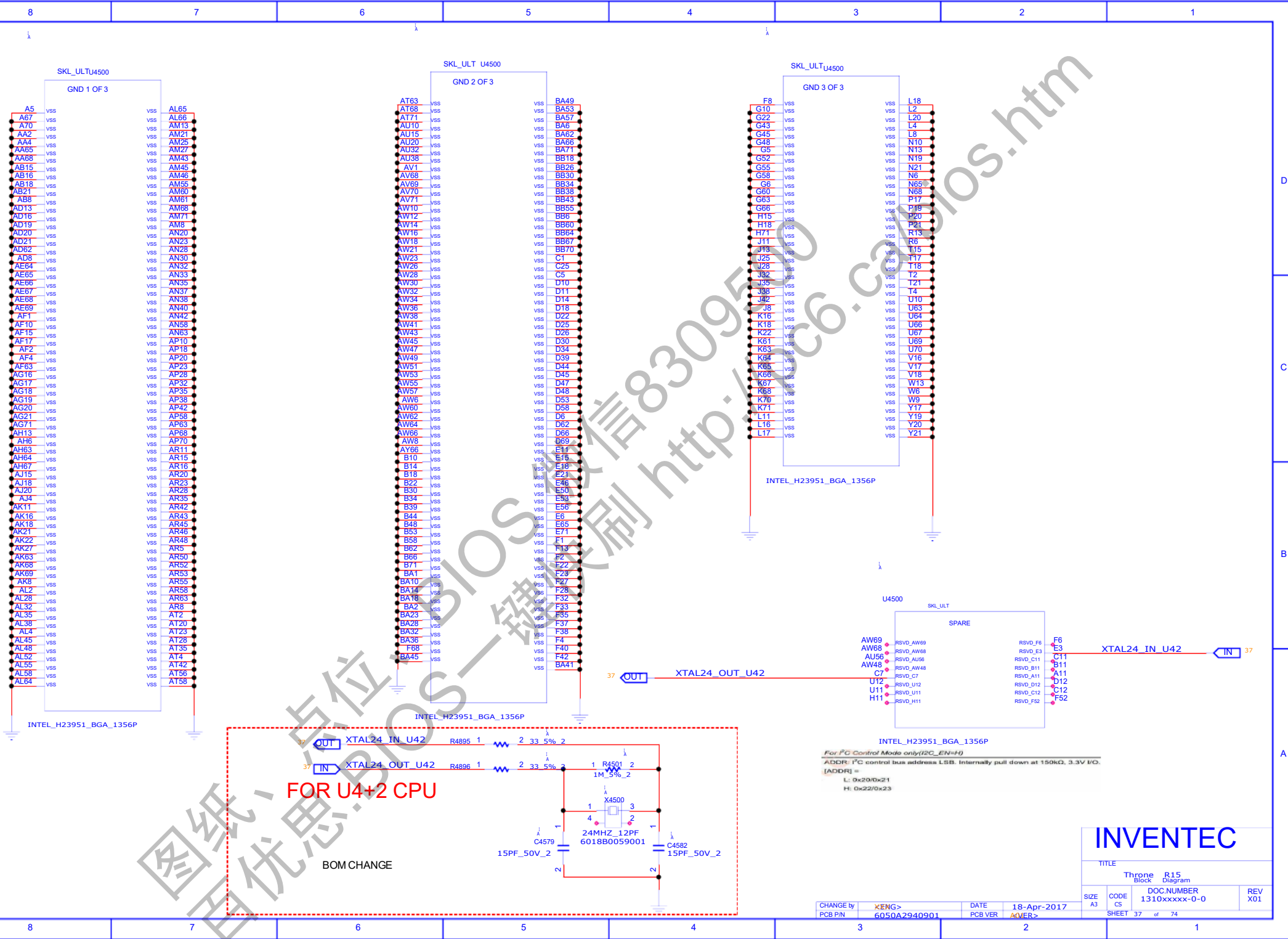
A

D

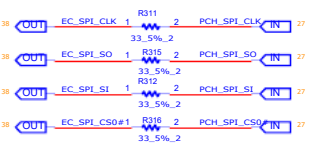
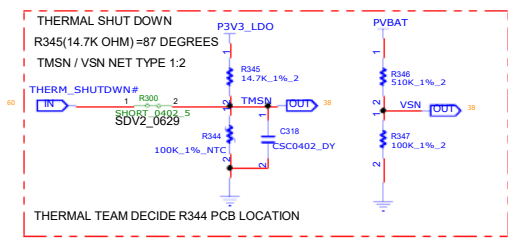
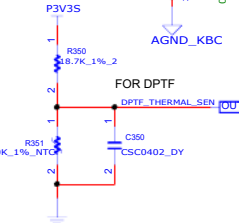
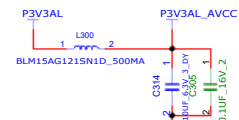
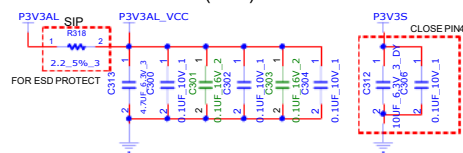
C

B

A

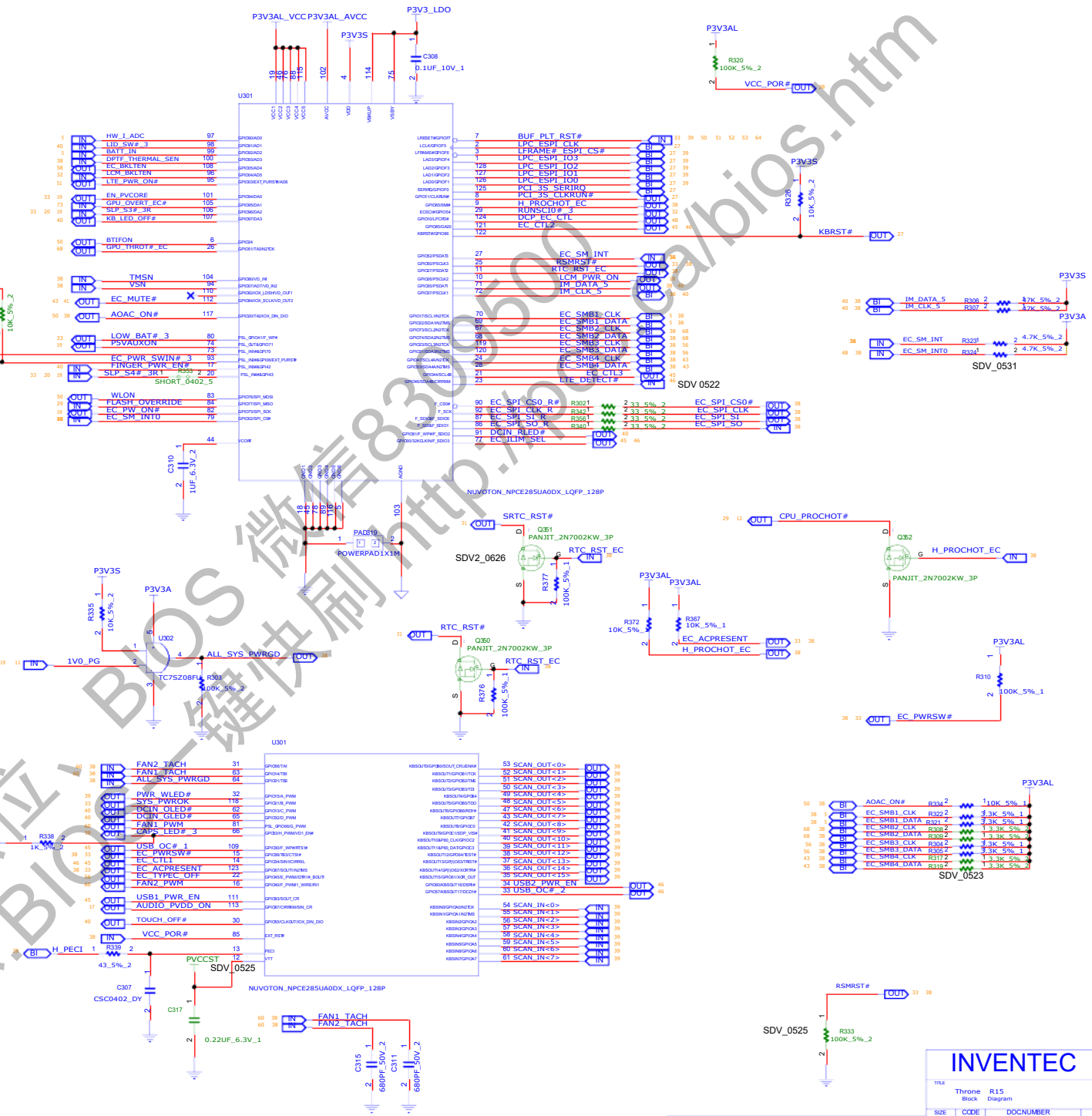
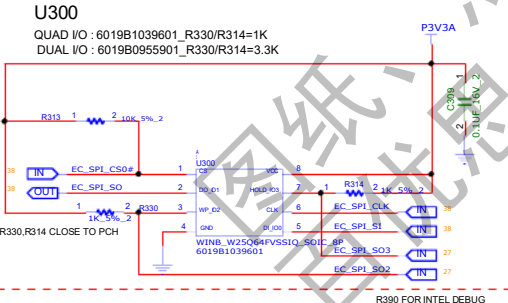


REFERENCE 300-389(KBC)



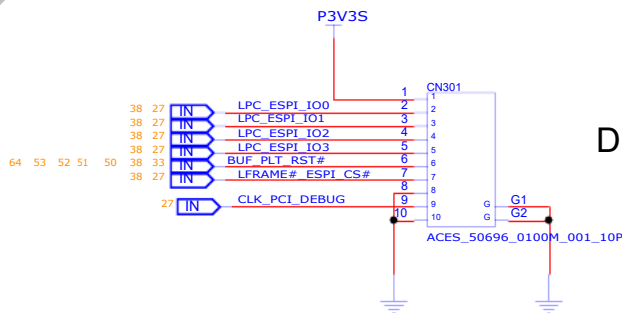
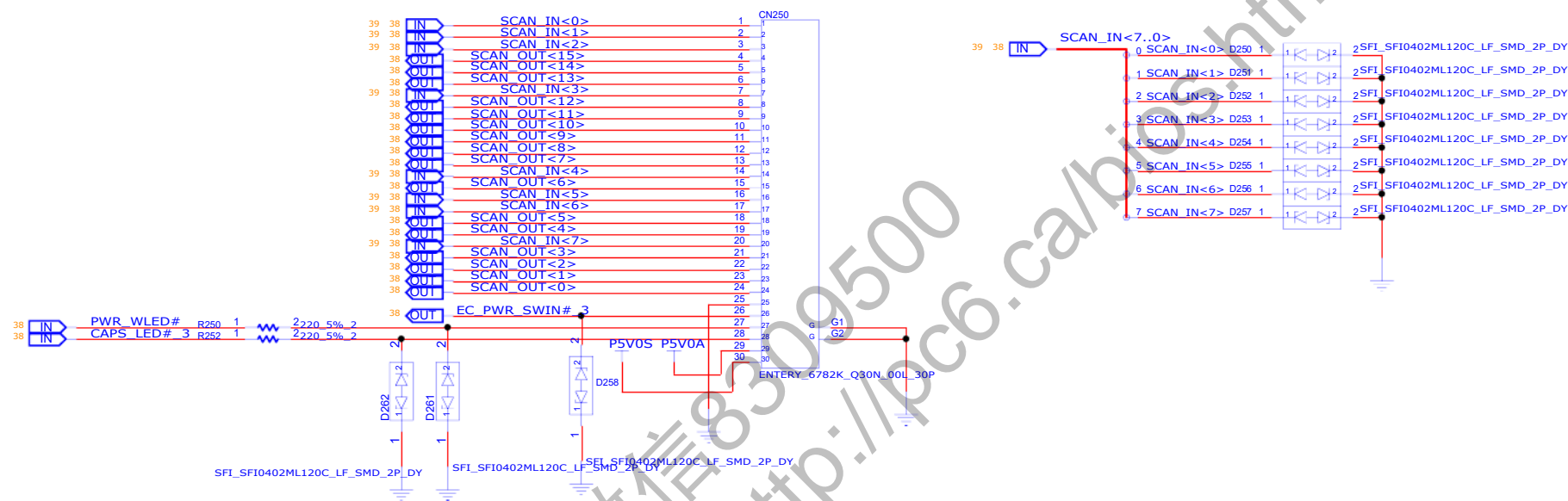
EC_SMB1	EC_SMB2	EC_SMB3	EC_SMB4
1.BATTERY	USB3 HUB	TYPE C	TI AMP
2.CHARGE	GPU	TYPE C P1	

ALL EC & PCH RESISTOR NEED TO WITHIN 0.5" OF ROM(U300)



INVENTEC

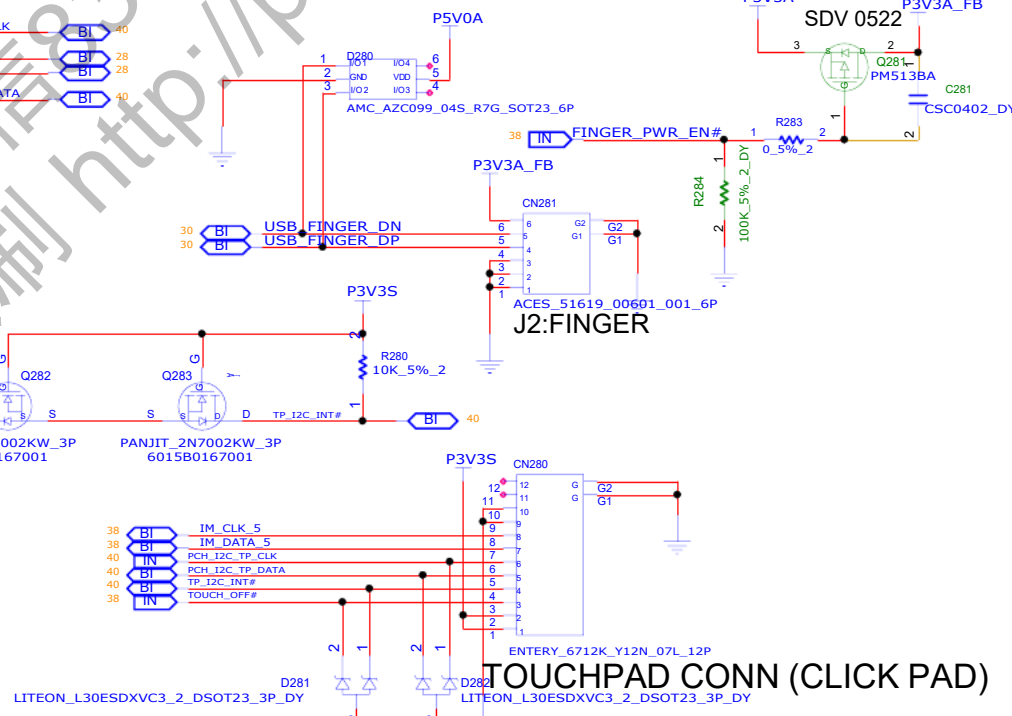
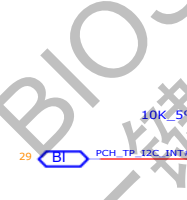
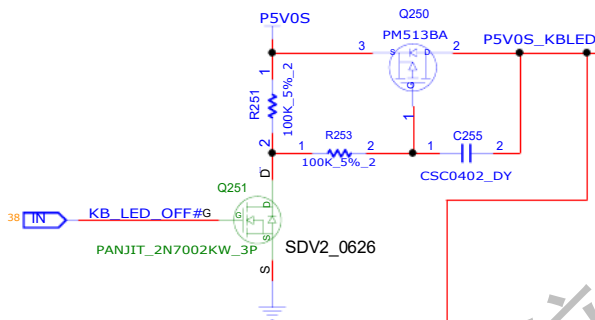
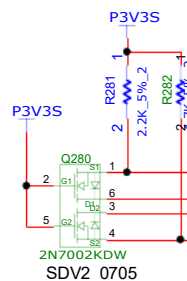
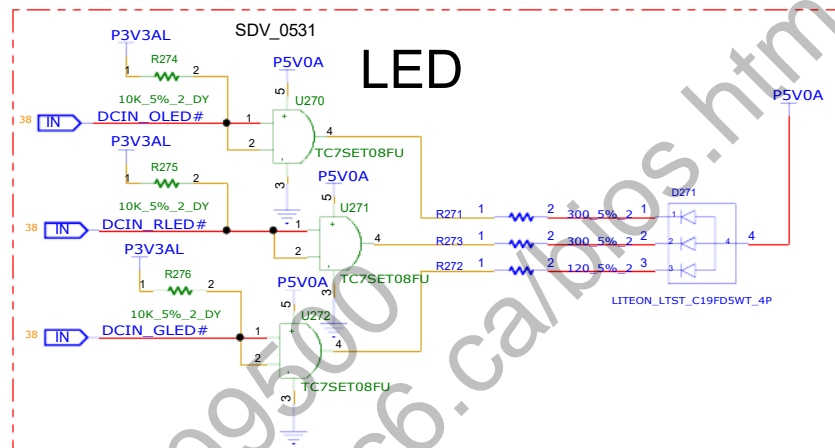
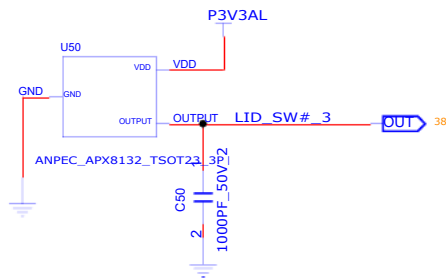
REFERENCE 200~249(POWER CONN)
REFERENCE 250~299(KB/TP CONN)



INVENTEC

TITLE			
Throne R15 Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01
SHEET	of 39	74	

CHANGE by XXX	DATE
PCB P/N 66NGA2940901	PCB VER A18-Apr-2017



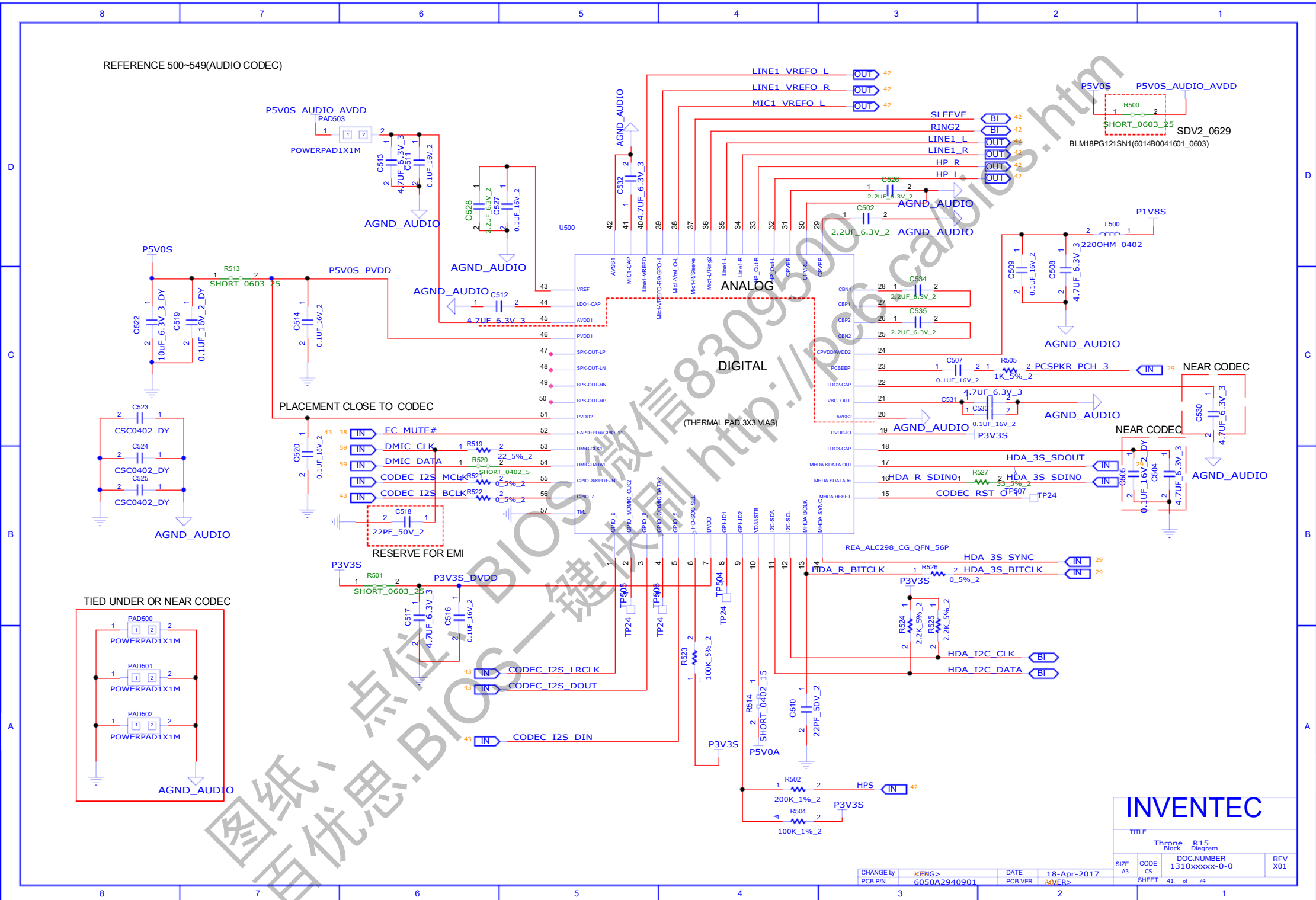
KEYBOARD LED CONN

TOUCHPAD CONN (CLICK PAD)

INVENTEC

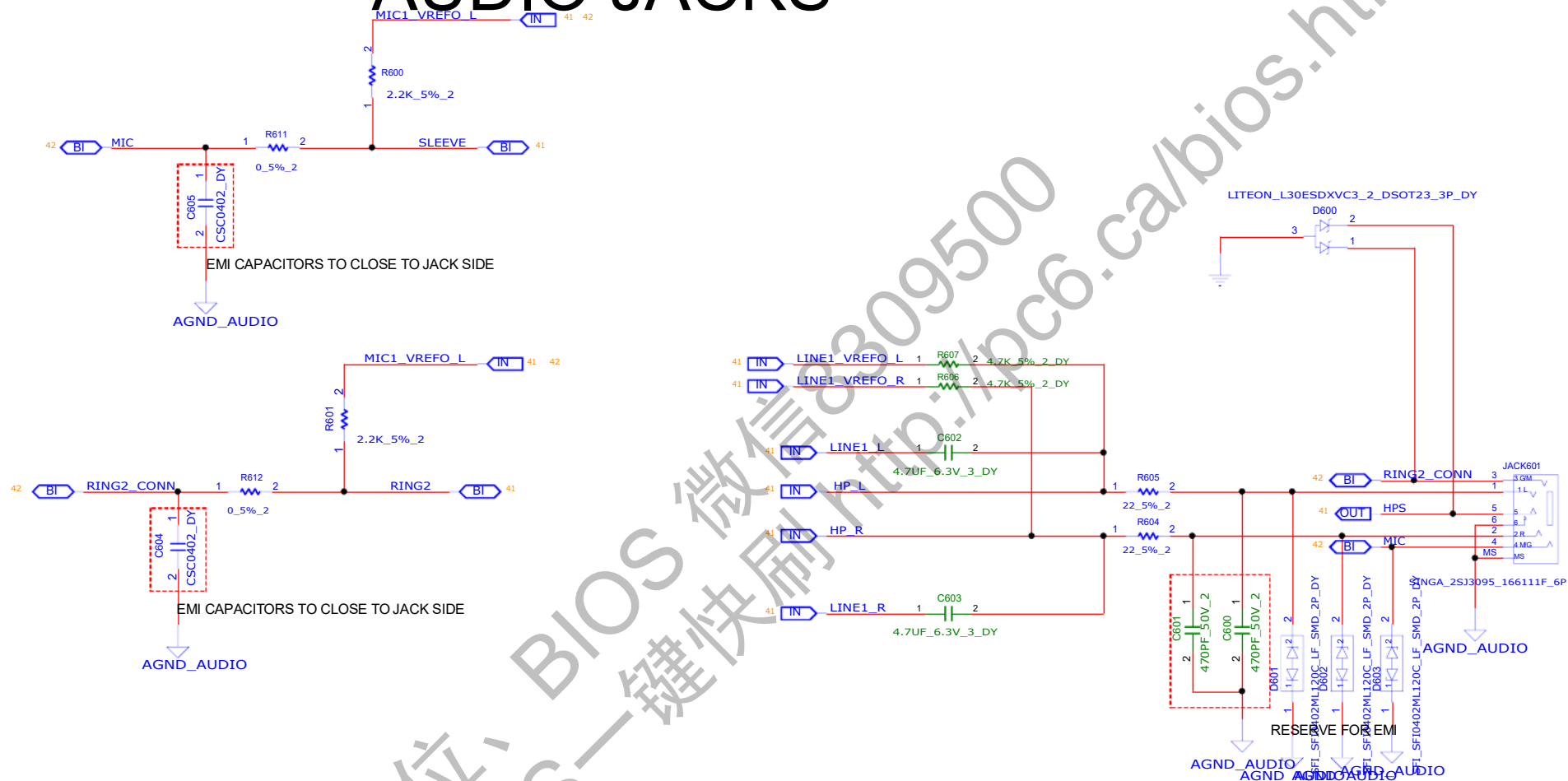
CHANGE BY	XXX	DATE	18-Apr-2017
PCB P/N	6050A2940901	PCB VER	A01
SHEET	40	of	74

TITLE	Throne R15 Block Diagram
SIZE	A3
CODE	CS
DOC NUMBER	1310xxxxx-0-0
REV	X01



REFERCE 600~649(JACK/MIC/SPEAKER)

AUDIO JACKS



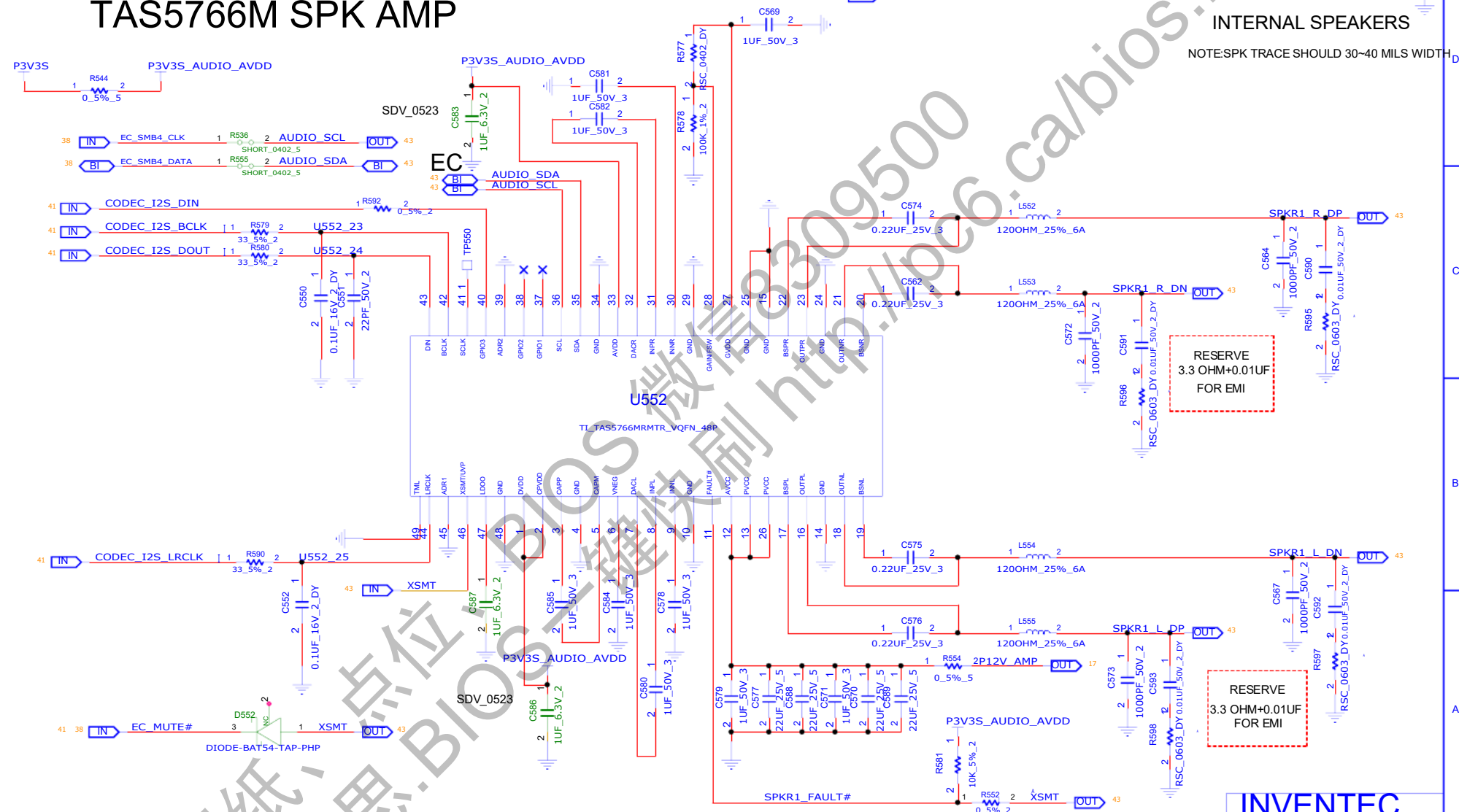
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TITLE			
Throne R15 Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET 42 of 74			

CHANGE by XXX	DATE 18-Apr-2017
PCB P/N 6050A2940901	PCB VER A01

SPEAKER AMP

TAS5766M SPK AMP



INTERNAL SPEAKERS

NOTE:SPK TRACE SHOULD 30~40 MILS WIDTH

RESERVE
3.3 OHM+0.01UF
FOR EMI

RESERVE
3.3 OHM+0.01UF
FOR EMI

INVENTEC

CHANGE BY	XXX	DATE	18-Apr-2017
PCB PN	6050A2940901	PCB VER	A01

TITLE	Throne R15 Block Diagram
SIZE	A3
CODE	CS
DOC NUMBER	1310xxxx-0-0
REV	X01
SHEET	43 of 74

CARD READER



SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET		44 of 74	

CHANGE by	XXX	DATE	18-Apr-2017
PCB P/N	6050A2940901	PCB VER	A01

USB 3.0 PORT1



TITLE
Throne Block R15 Diagram

DOC.NUMBER
1310xxxxx-0-0

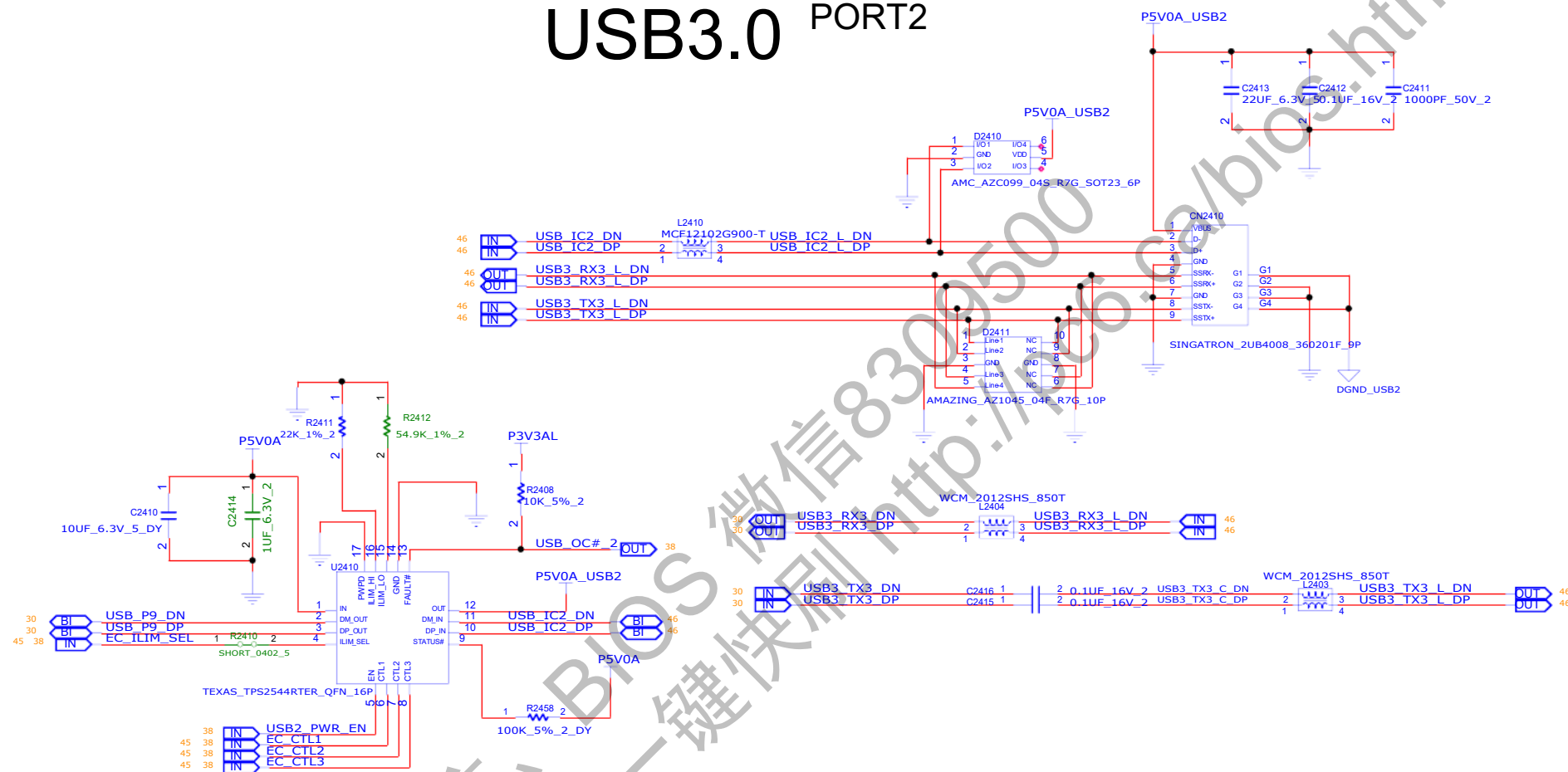
15100000 0 0

45 of 74

REV
X01

CHANGE by	XXX	DATE	18-Apr-2017
PCB P/N	6050A2940901	PCB VER	A01

USB3.0 PORT2



INVENTEC

TITLE			
Throne R15 Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01
SHEET	46	of 74	

CHANGE by	XXX	DATE	18-Apr-2017
PCB P/N	6050A2940901	PCB VER	A01

REFERENCE 2600~2699(USB RESERVE)



TITLE

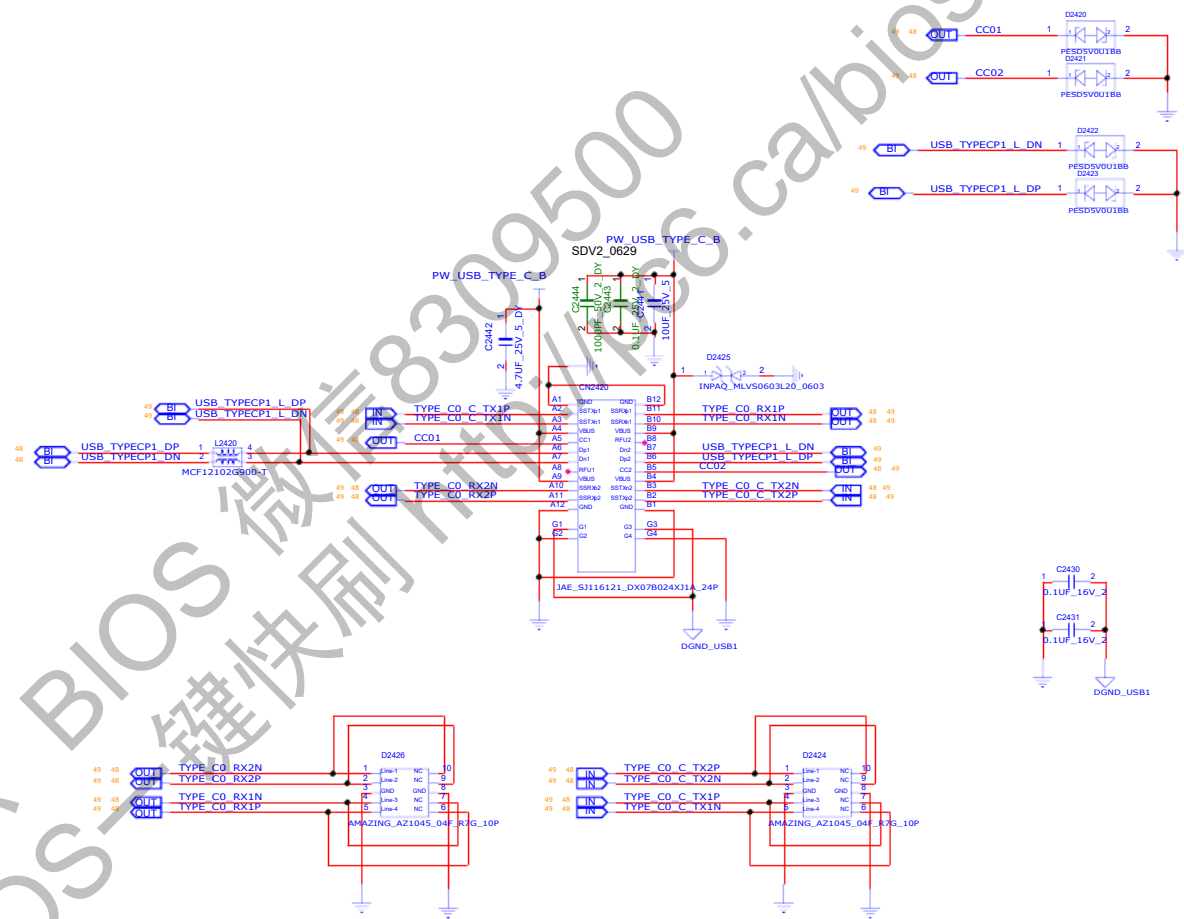
Throne Block R15 Diagram

SIZE A3	CODE CS	DOC. NUMBER 1310xxxxx-0-0	REV X01
SHEET		47 of 74	

CHANGE by	XXX	DATE	18-Apr-2017
PCB P/N	6050A2940901	PCB VER	A01

A	
B	
C	
D	
E	
F	

CBA



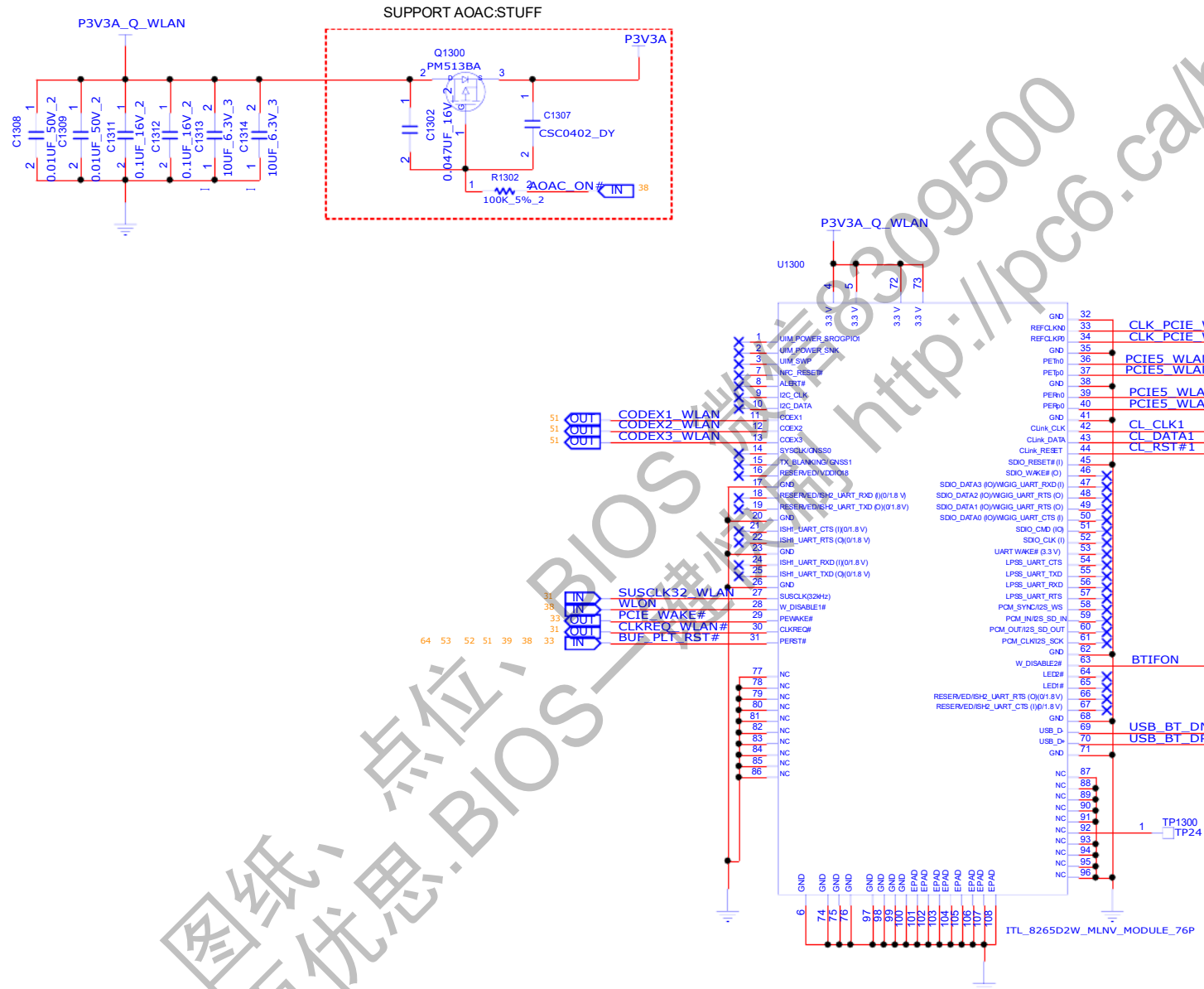
INVENTEC

TITLE			
Throne R15			

SIZE	CODE	DOCUMENT	REV
C	C5	1310xxxx-0-0	X01
SHEET		of 49	24

CHANGE BY: XXXX DATE: 18-Apr-2017
PCB PIN: 6050A2940901 PCB VER: A5VER>

WLAN
REFERENCE 1300 ~ 1349



INVENTEC

TITLE
Throne R15
Block Diagram

CHANGE by
PCB P/N

XXX
6050A2940901

DATE
PCB VER

18-Apr-2017
A01

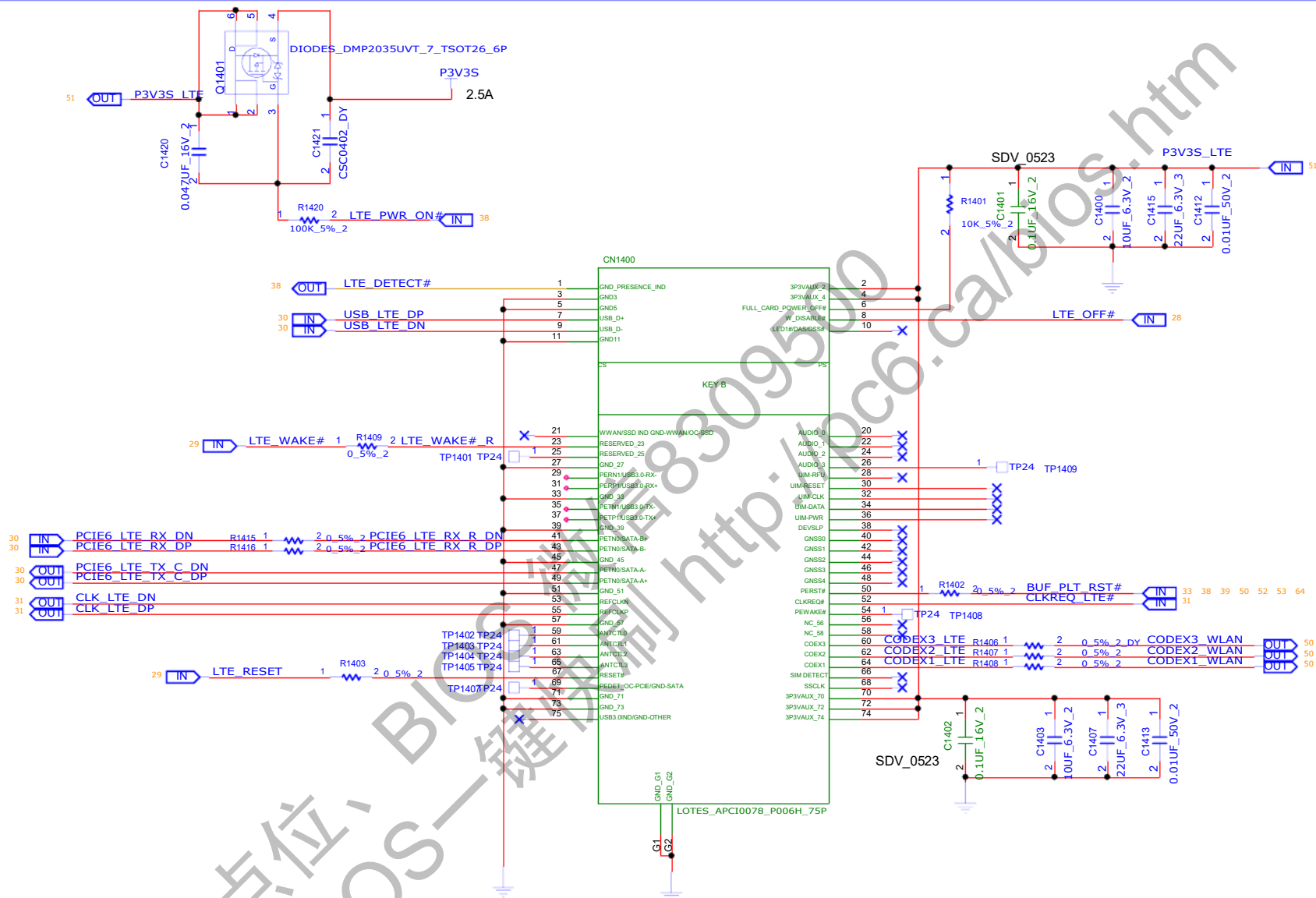
DOC NUMBER
1310xxxxx-0-0

REV
X01

SHEET
50 of 74

4G_LTE

REFERENCE 1400~1499(4G)



INVENTEC

Throne R15
Diagram

DOC NUMBER
1310xxxx-0-0

REV
X01

CHANGE by XXX
PCB P/N 6RNGA2940901
DATE
PCB VER A18-Apr-2017

SIZE A3
CODE CS
SHEET of 51 74

D

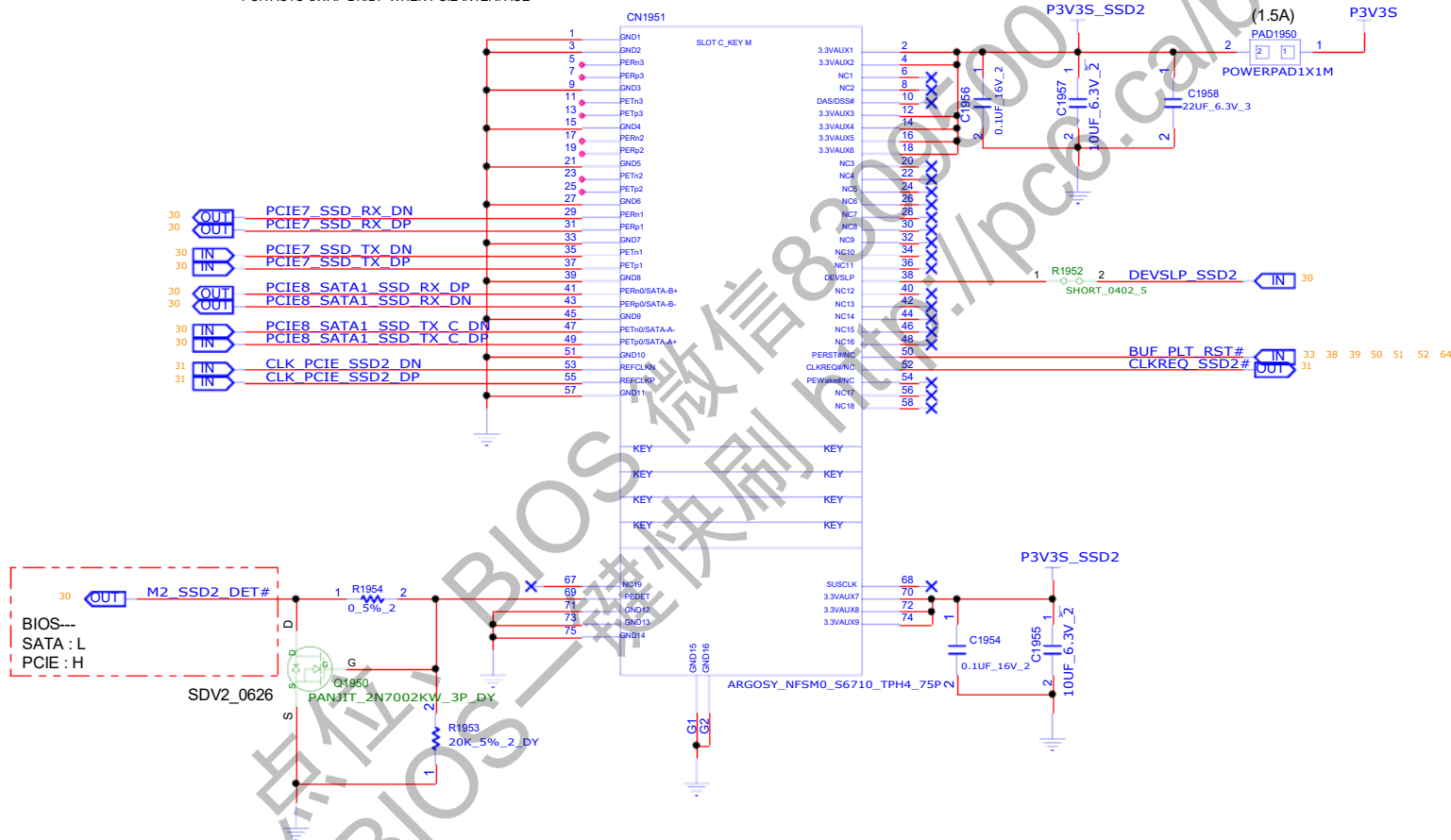


B

A

NGFF SSD2(PCIE/SATA 2X)

PCH AUTO SWAP DN/DP WHEN PCIE INTERFACE



M.2 CARD USES; SATA SIGNALING (LOW) OR PCIE SIGNALING (HIGH)

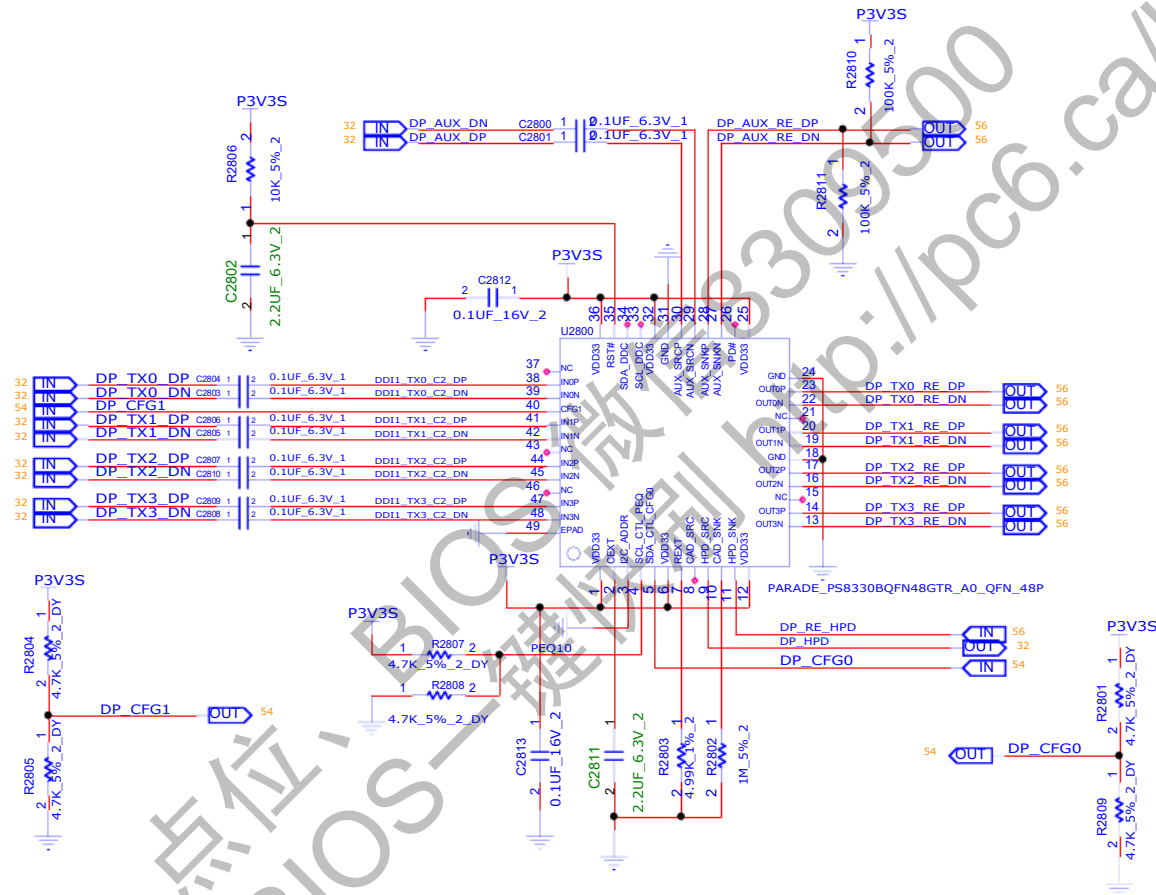
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INVENTEC

TITLE			
Throne Block R15 Diagram			
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SHEET	53	of 74	

CHANGE by	XXX	DATE	18-Apr-2017
PCB P/N	6050A2940901	PCB VER	A01

DP REDRIVER



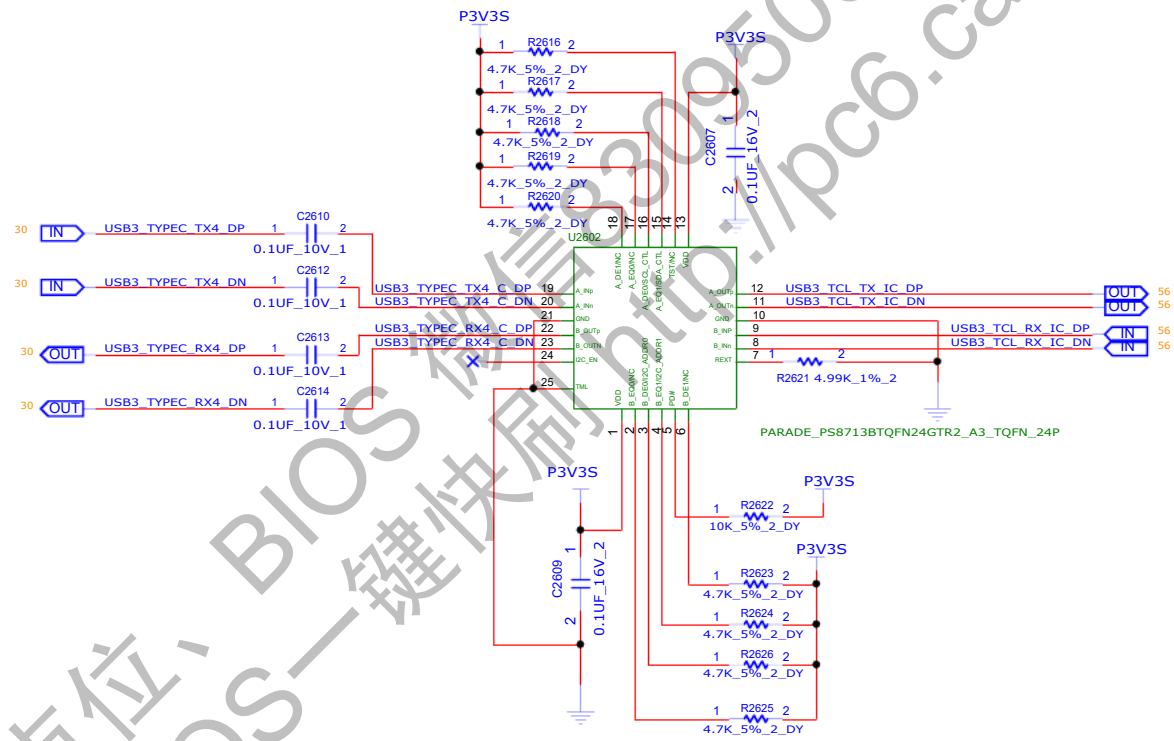
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SHEET 54 of 74			

CHANGE by	XXX	DATE	18-Apr-2017
PCB P/N	6050A2940901	PCB VER	A01

USB3 REDRIVER

REFERENCE 2600~2699(USB RESERVE)



INVENTEC

TITLE			
Throne Block R15 Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET 55	of 74		

CHANGE by XXX	DATE 18-Apr-2017
PCB P/N 6050A2940901	PCB VER A01

3.3V MODE	5V MODE	
R2602	V	OPEN
R2698	OPEN	V
Q2691	OPEN	V
R2600	V	OPEN

Slave Addr	Ra 1%	Rb 1%
addr0	NC	10K
addr1	54.9K	12.1K
addr2	27.4K	15.8K
addr3	18.2K	22.1K

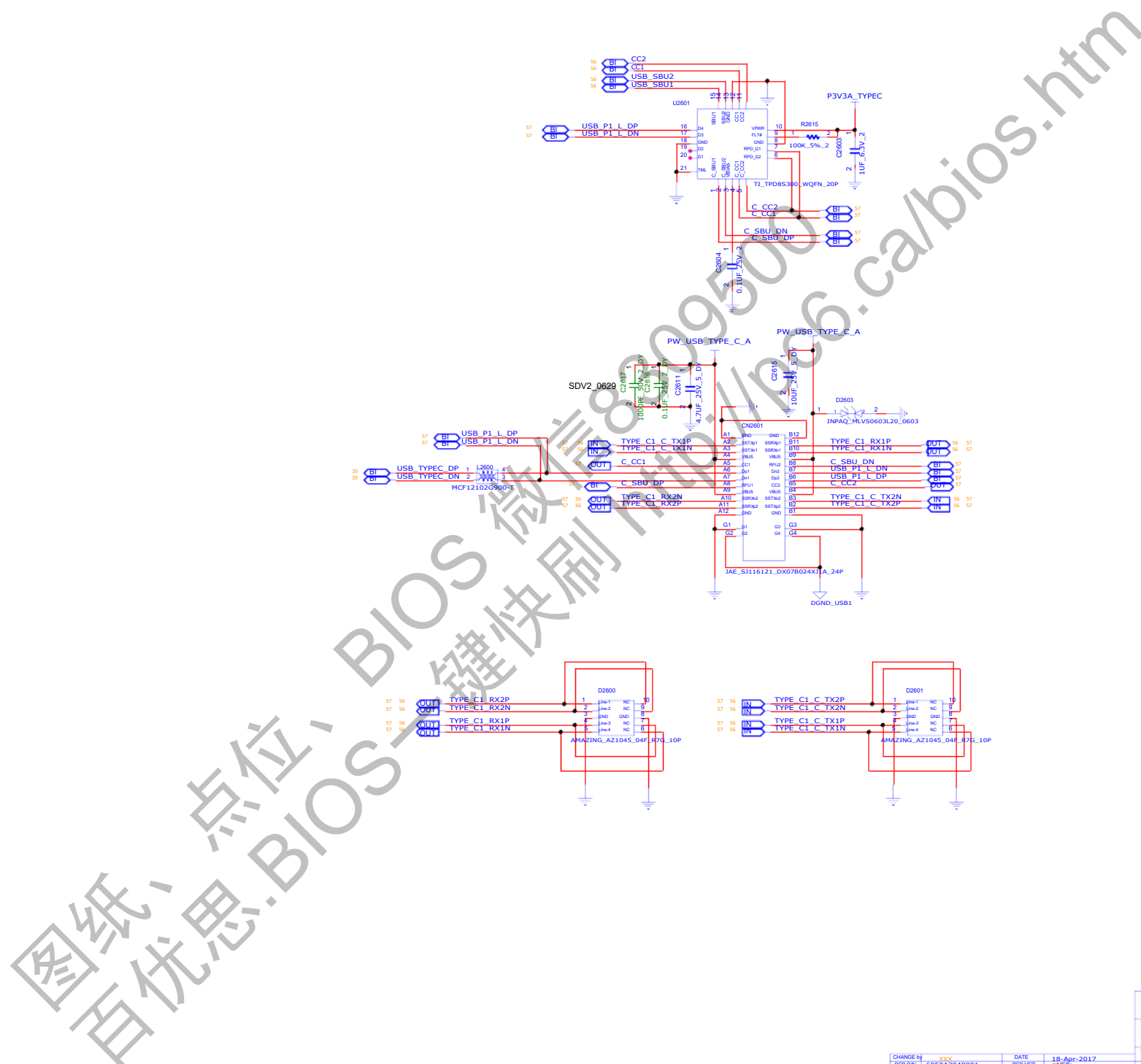
Truth Table

SEL	OE	Y+	Y-
X	H	Hi-Z	Hi-Z
L	L	M+	M+
H	L	D+	D+

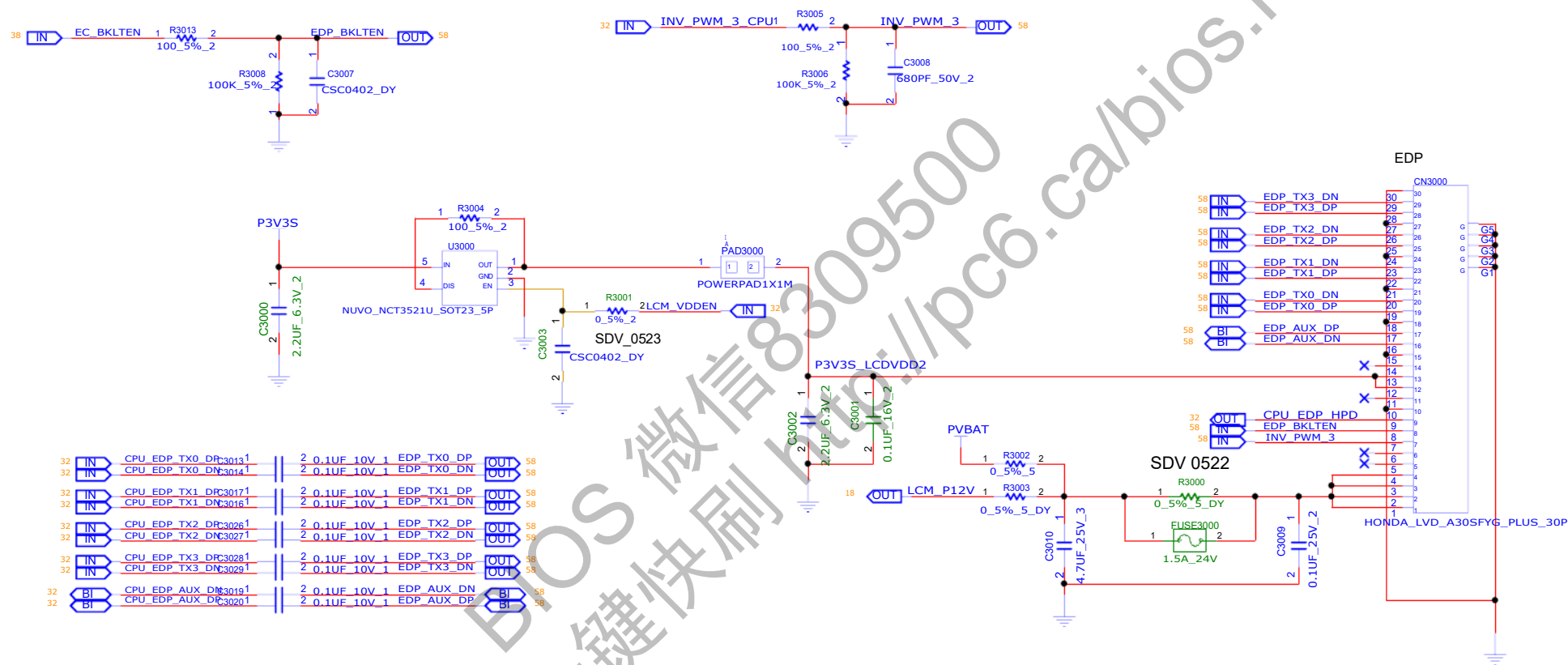
INVENTEC

TITLE	Throne R15
SIZE	TPS5450
CODE	CS
REV	X01
DOC NUMBER	1310xxxxx-0-0
SHEET	56
of	24

CHANGE BY: XXXX DATE: 18-Apr-2017
PCB PIN: 6050A2940901 PCB VER: AVER>



EDP CONN



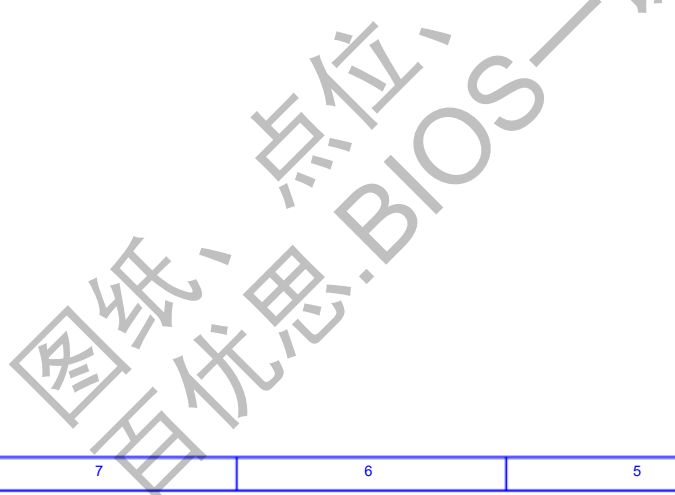
INVENTEC

Throne
Block Diagram

R15

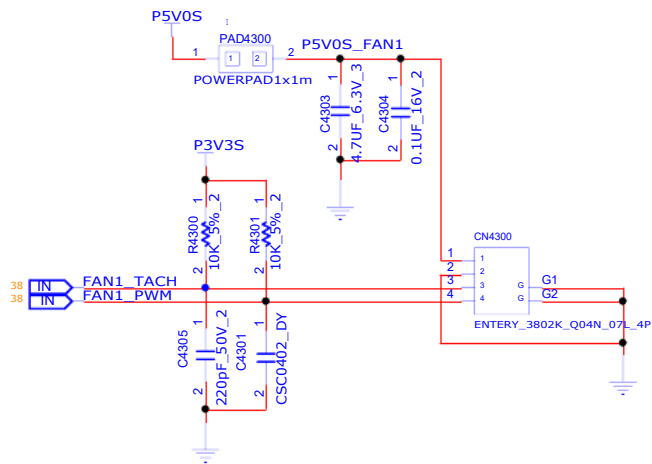
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PCB P/N 6050A2940901
DATE 18-Apr-2017
PCB VER A01SIZE A3
CODE CS
SHEET 58 of 74

A

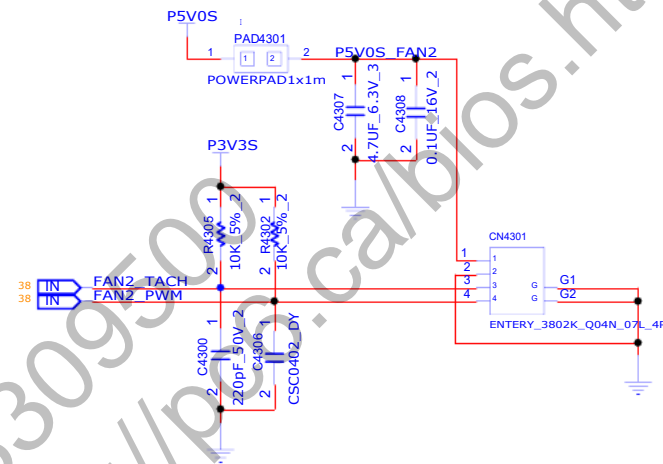


CHANGE by	XXX	DATE	18-Apr-2017
PCB P/N	6050A2940901	PCB VER	A01

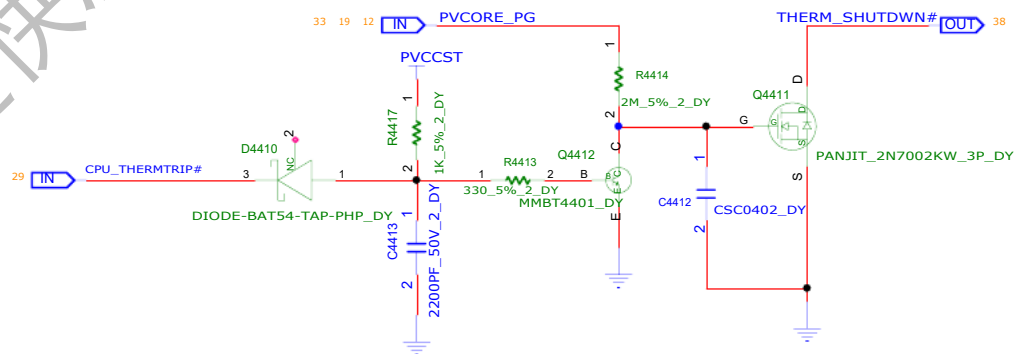
REFERENCE 4300~4349(FAN)
REFERENCE 4411~4449(THERMAL)



FAN1 CN CPU



FAN2 CN CPU



REFERENCE NUMBER:4411~4449

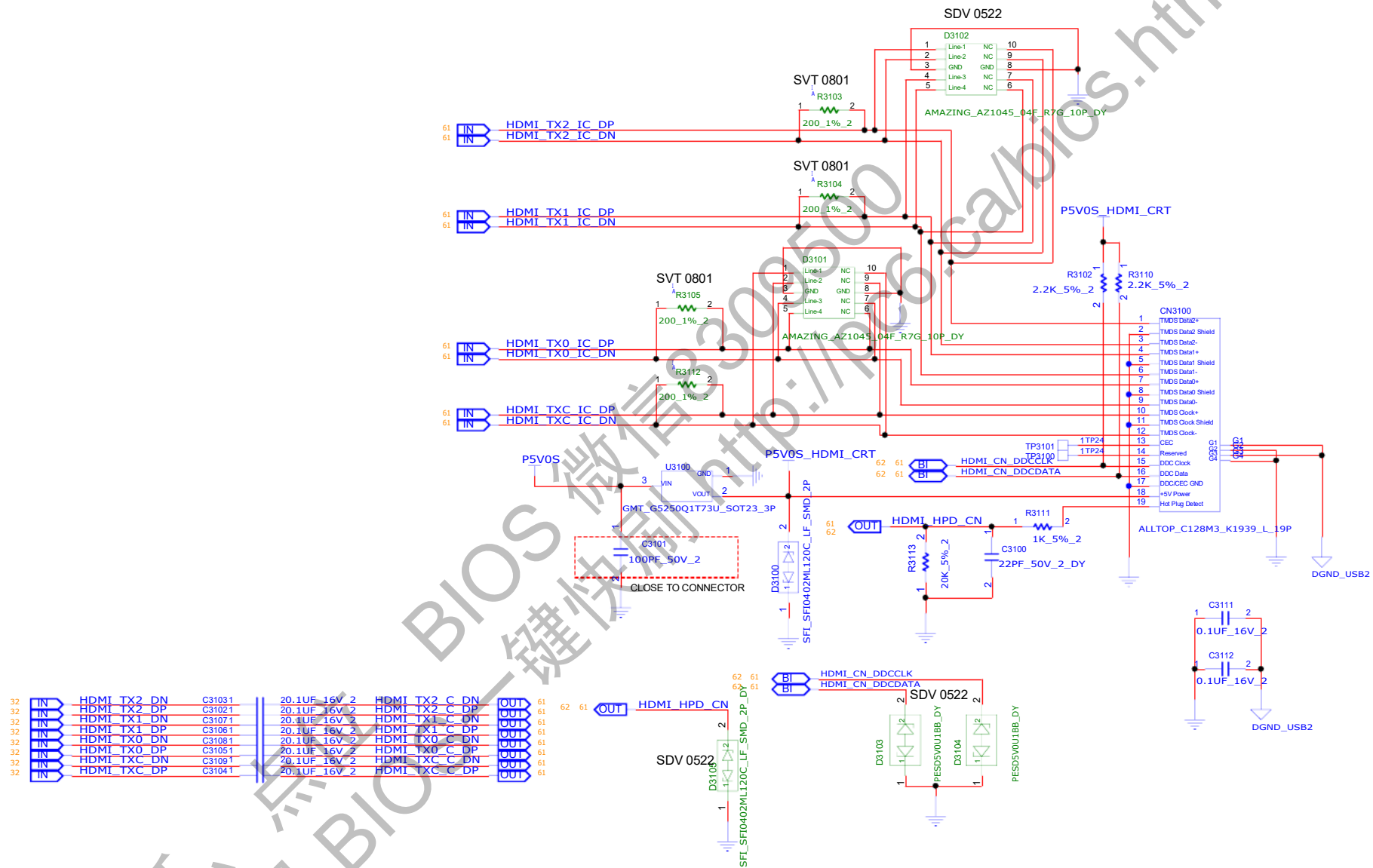
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TITLE		Throne R15 Diagram	
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET	of 60	74	

CHANGE by XXX	DATE
PCB P/N 6FNGA2940901	PCB VER A18-Apr-2017



CHANGE by	XXX	DATE	18-Apr-2017
PCB P/N	6050A2940901	PCB VER	A01



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TITLE
Throne R15
Diagram

DOC NUMBER
1310xxxx-0-0

REV
X01

CHANGE by XXX 6050A2940901 DATE 18-Apr-2017 PCB VER A01

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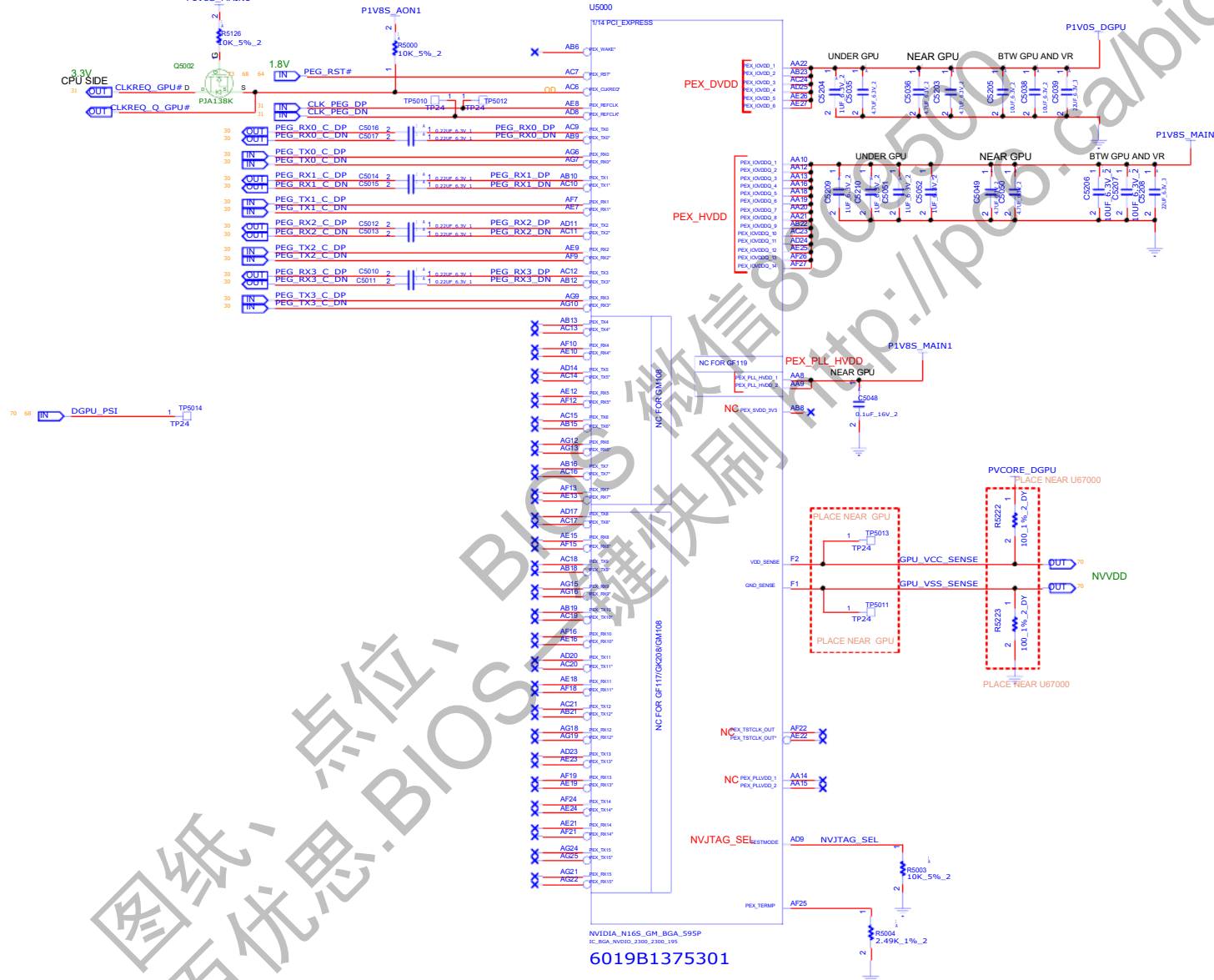
NOTES:
1.HSF Property: Comply iSupplier system HSF property attribute up-to-date value.

N17S-LG
GDDR5 23X23

2017.08.09

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DATE	CHANGE NO.	REV

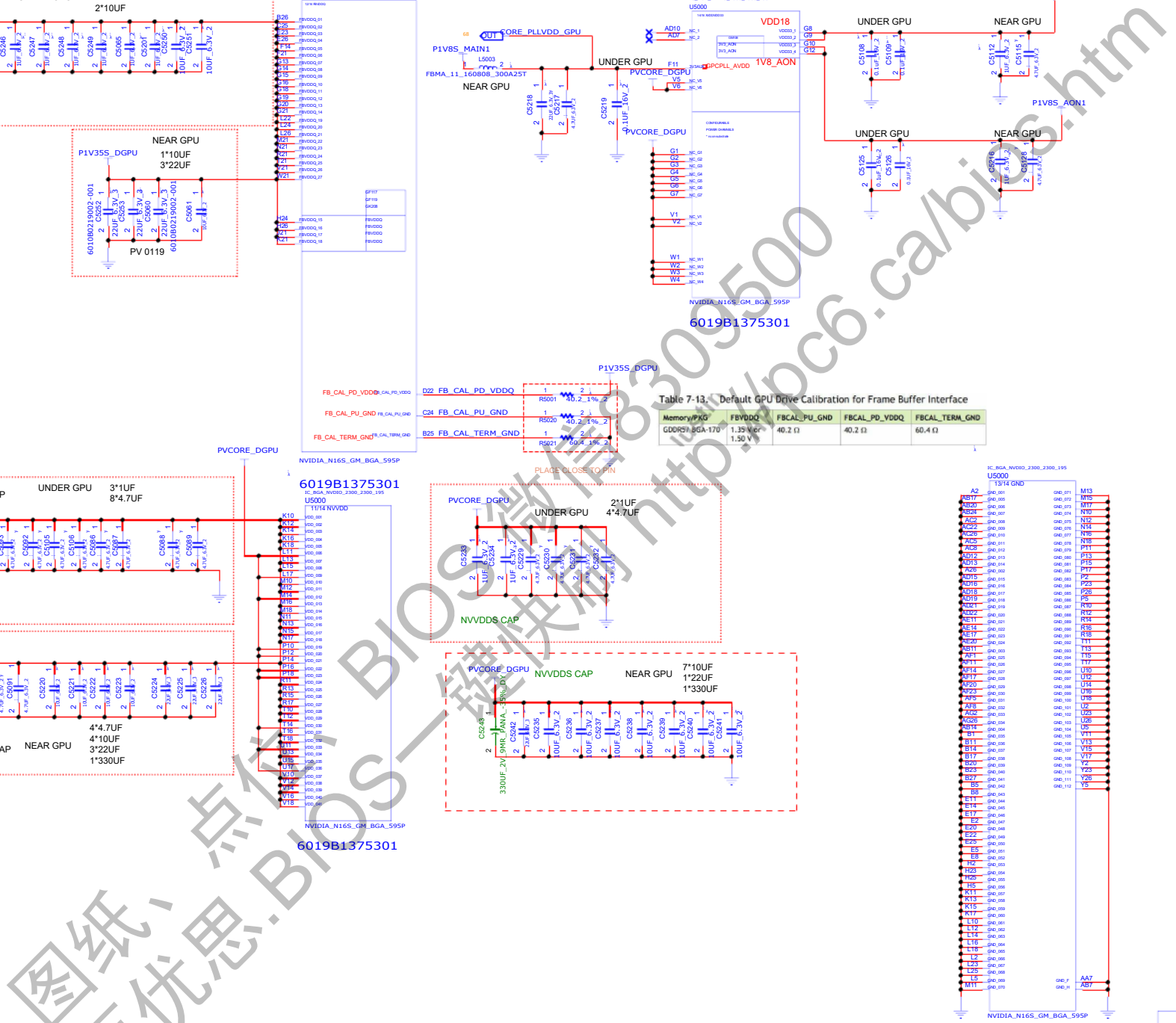
Chan, Share Huang, Vens			Shiu, Vini		INVENTEC				
DESIGN / DRAWER			DATE		TITLE				
CHECK			18-Apr-2017		Throne R15				
APPROVAL			A01		SIZE				
FILE NAME			PCB VER		CODE		DOC NUMBER		REV
PCB PIN			A01		SHEET		1310xxxxx-0-0		X01
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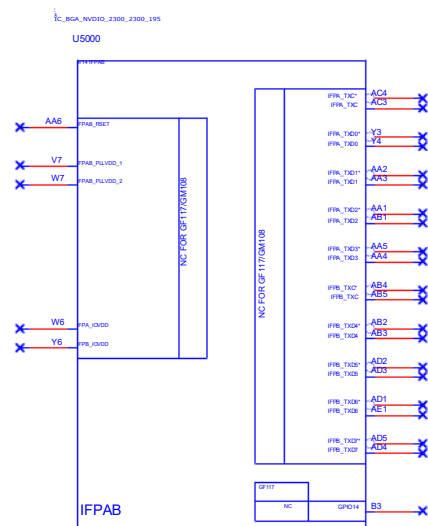


Notes:

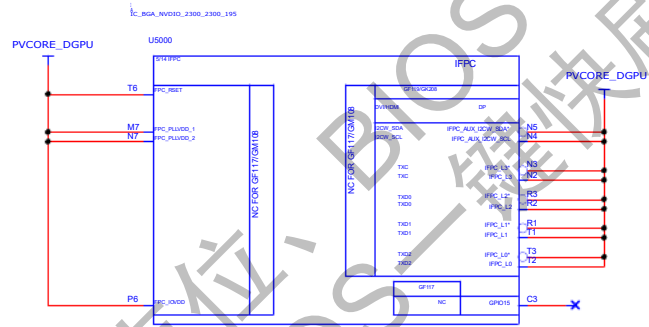
1. Not available in GB2-64 and GB2B-64 packages.



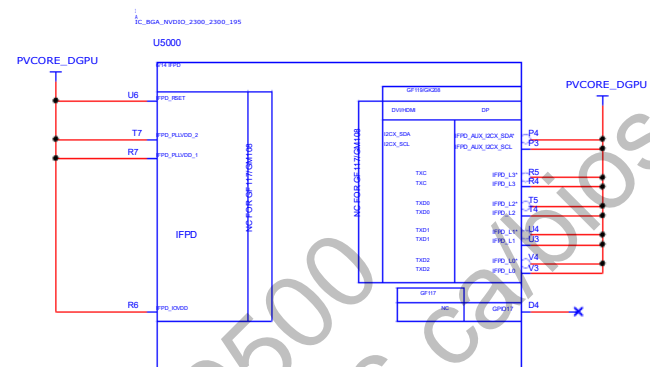




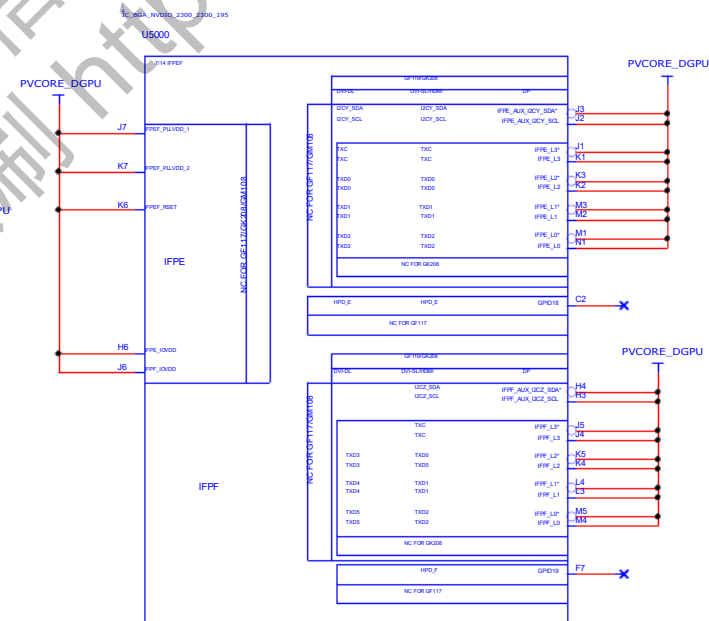
NVIDIA_N16S_GM_BGA_595P
6019B1375301



NVIDIA_N16S_GM_BGA_595P
6019B1375301



NVIDIA_N16S_GM_BGA_595P
6019B1375301



NVIDIA_N16S_GM_BGA_595P
6019B1375301

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TITLE		Throne R15	
GPU-4		GPU-4	
SIZE	CODE	DOCNUMBER	REV
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PCB PN	6050A2940501	PCB VER	A01

Physical Strapping Pin	GPU	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCL	N155-GH-07 N155-GH-07 All Q82-A4 N14 and Q84-A15	PCL_DEV0[3] S0RL_DEV0[3]	S0BL_DEV0[0] S0RL_DEV0[0]	PCL_DEV0[1] S0RL_DEV0[1]	PCL_PLL_CLK_TEN[0] S0BL_DEV0[0]
ROM_S1	N155-GH-07 N14 and Q84-A15	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_S0	N155-GH-07 N155-GH-07	FR[1] DEVID_SEL	FR[0] P_CIE_CFG	SMB_ADDR_ADDR	VGA_DEVICE
STRAP0	N155-GH-07 N155-GH-07	USER[3] Reserved (keep pull-up and pull-down footprints and leave them not stubbed by default)	USER[2] Reserved (keep pull-up and pull-down footprints and leave them not stubbed by default)	USER[1] Reserved (keep pull-up and pull-down footprints and leave them not stubbed by default)	USER[0] Reserved (keep pull-up and pull-down footprints and leave them not stubbed by default)
STRAP1	N155-GH-07 N155-GH-07	S0RL_DEV0[3] Reserved (keep pull-up and pull-down footprints and leave them not stubbed by default)	S0BL_DEV0[3] Reserved (keep pull-up and pull-down footprints and leave them not stubbed by default)	S0RL_DEV0[1] Reserved (keep pull-up and pull-down footprints and leave them not stubbed by default)	S0BL_DEV0[1] Reserved (keep pull-up and pull-down footprints and leave them not stubbed by default)
STRAP2	N155-GH-07 N155-GH-07	PCL_DEV0[3] Reserved (keep pull-up and pull-down footprints and leave them not stubbed by default)	PCL_DEV0[2] Reserved (keep pull-up and pull-down footprints and leave them not stubbed by default)	PCL_DEV0[1] Reserved (keep pull-up and pull-down footprints and leave them not stubbed by default)	PCL_DEV0[0] Reserved (keep pull-up and pull-down footprints and leave them not stubbed by default)
STRAP3	N155-GH-07 N155-GH-07	S0RL_DEV0[3] Reserved (keep pull-up and pull-down footprints and leave them not stubbed by default)	S0BL_DEV0[3] Reserved (keep pull-up and pull-down footprints and leave them not stubbed by default)	S0RL_DEV0[1] Reserved (keep pull-up and pull-down footprints and leave them not stubbed by default)	S0BL_DEV0[1] Reserved (keep pull-up and pull-down footprints and leave them not stubbed by default)
STRAP4	N155-GH-07 N155-GH-07	PCL_DEV0[3] Reserved (keep pull-up and pull-down footprints and leave them not stubbed by default)	P_CIE_SPEED_CFG NGL_DEV0_CFG	PCL_MAX_SPEED NGL_DEV0_CFG	PDLL_VDD33V Reserved (keep pull-up and pull-down footprints and leave them not stubbed by default)

This strap selects the pre-programmed Device IDs inside the NVIDIA GPU, replacing the PCI_DEVICE straps. (This strap only exists in the GB2E-64 and GB4B-128 package GPUs. Set this strap to 0 by default. Please refer to the latest GPU specific Platform Update Notification for the latest configuration.

This strap selects the pre-programmed PCIe settings inside the NVIDIA GPU, replacing 3GIO_PADCFG. This strap only exists in the GM204 and GM208 package GPUs. Set this strap to 0 by default. Please refer to the latest GPU specific Platform Update Notification for the latest configuration.

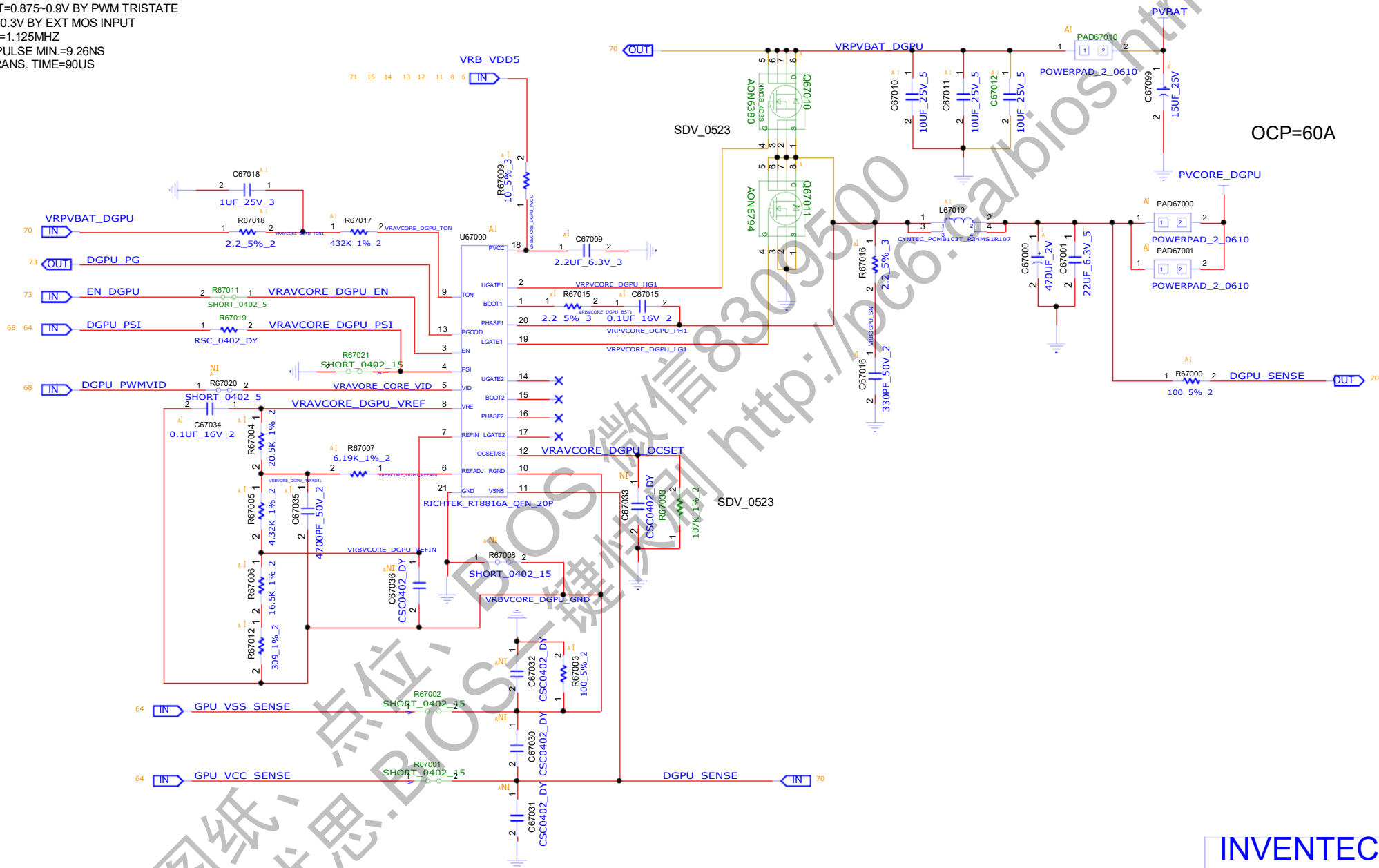
Strap Pins <small>see Note</small>			RANCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	M	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)



M3=U5500
NON MIRROR



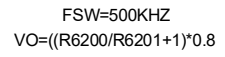
VMAX=1.2V BY PWM D=100%
 VMIN=0.6V PWM D=0%
 VBOOT=0.875-0.9V BY PWM TRISTATE
 VSTB=0.3V BY EXT MOS INPUT
 FPWM=1.125MHZ
 PWM PULSE MIN.=9.26NS
 VID TRANS. TIME=90US

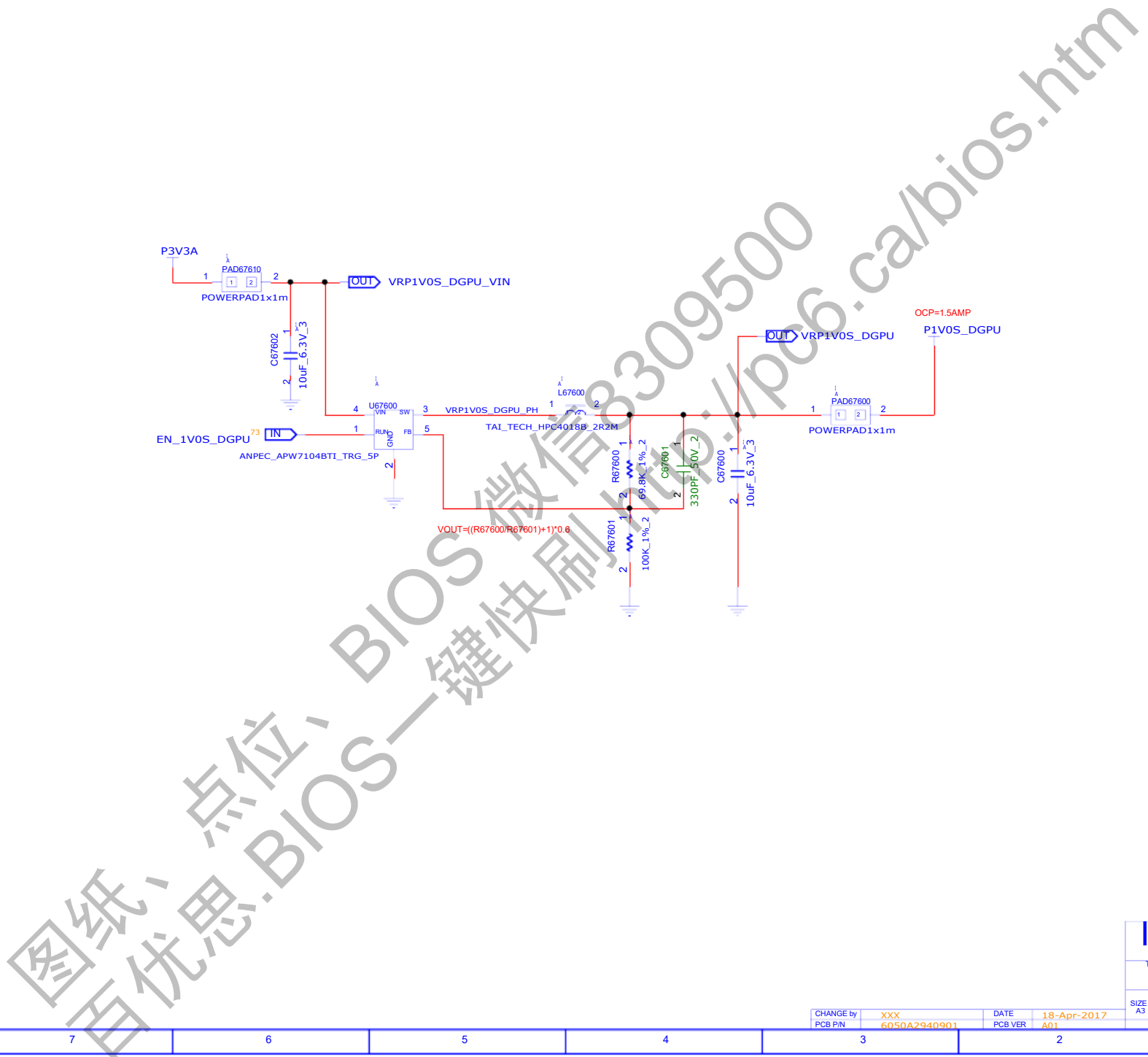


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TITLE			
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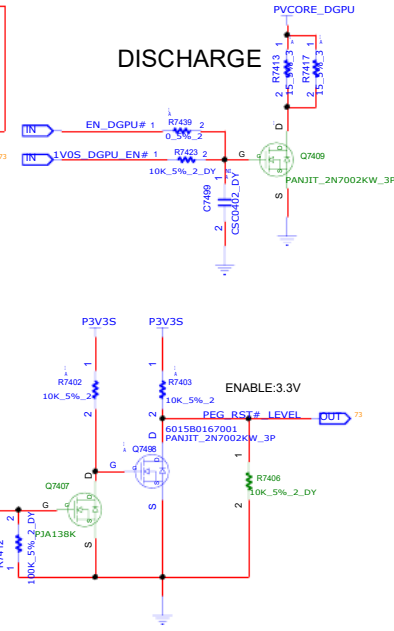
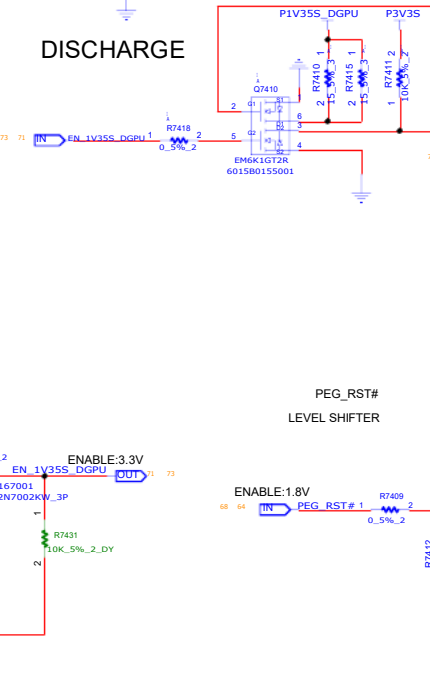
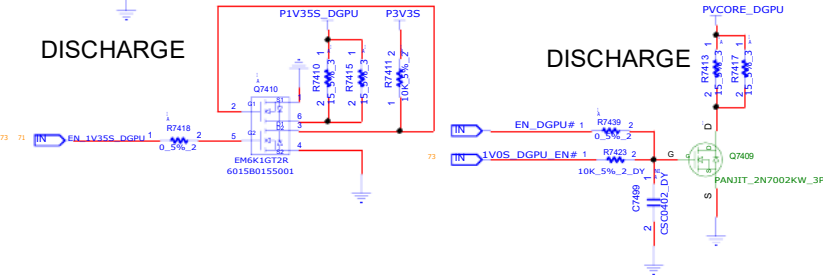
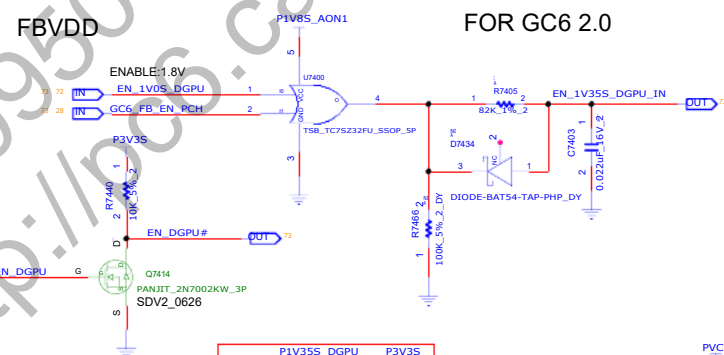
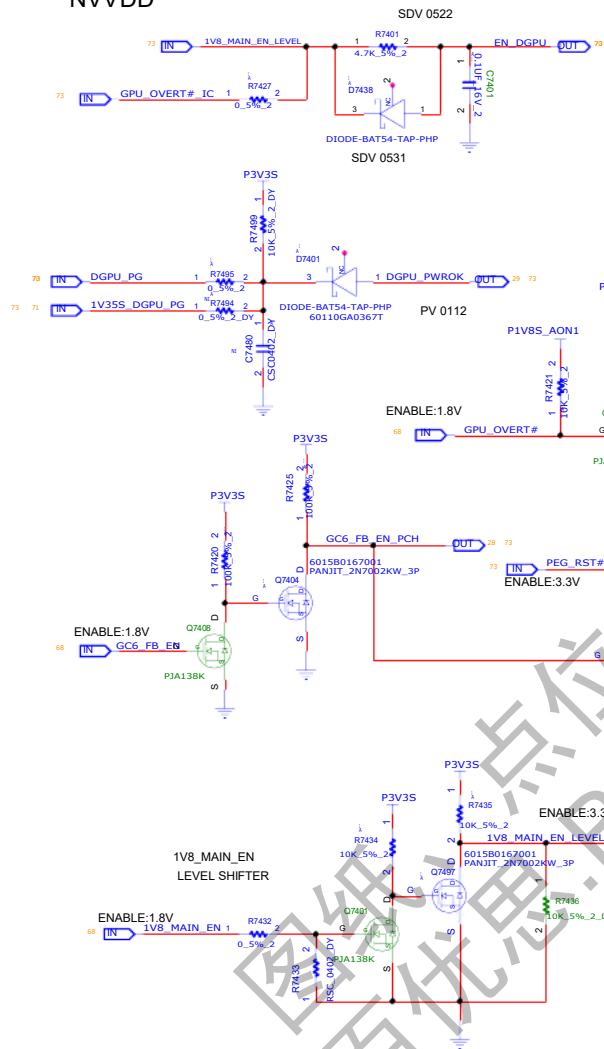
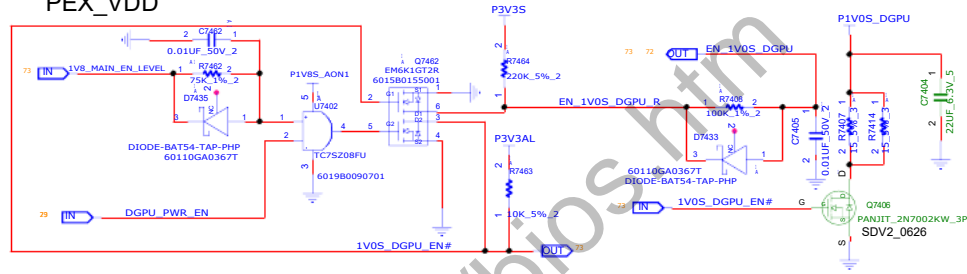
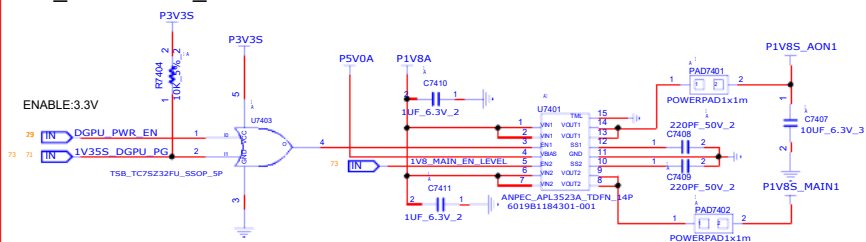
Throne Block R15 Diagram

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Throne R15 Block Diagram		
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